Microcontroller Programming

Atmel ATmega8/128/328

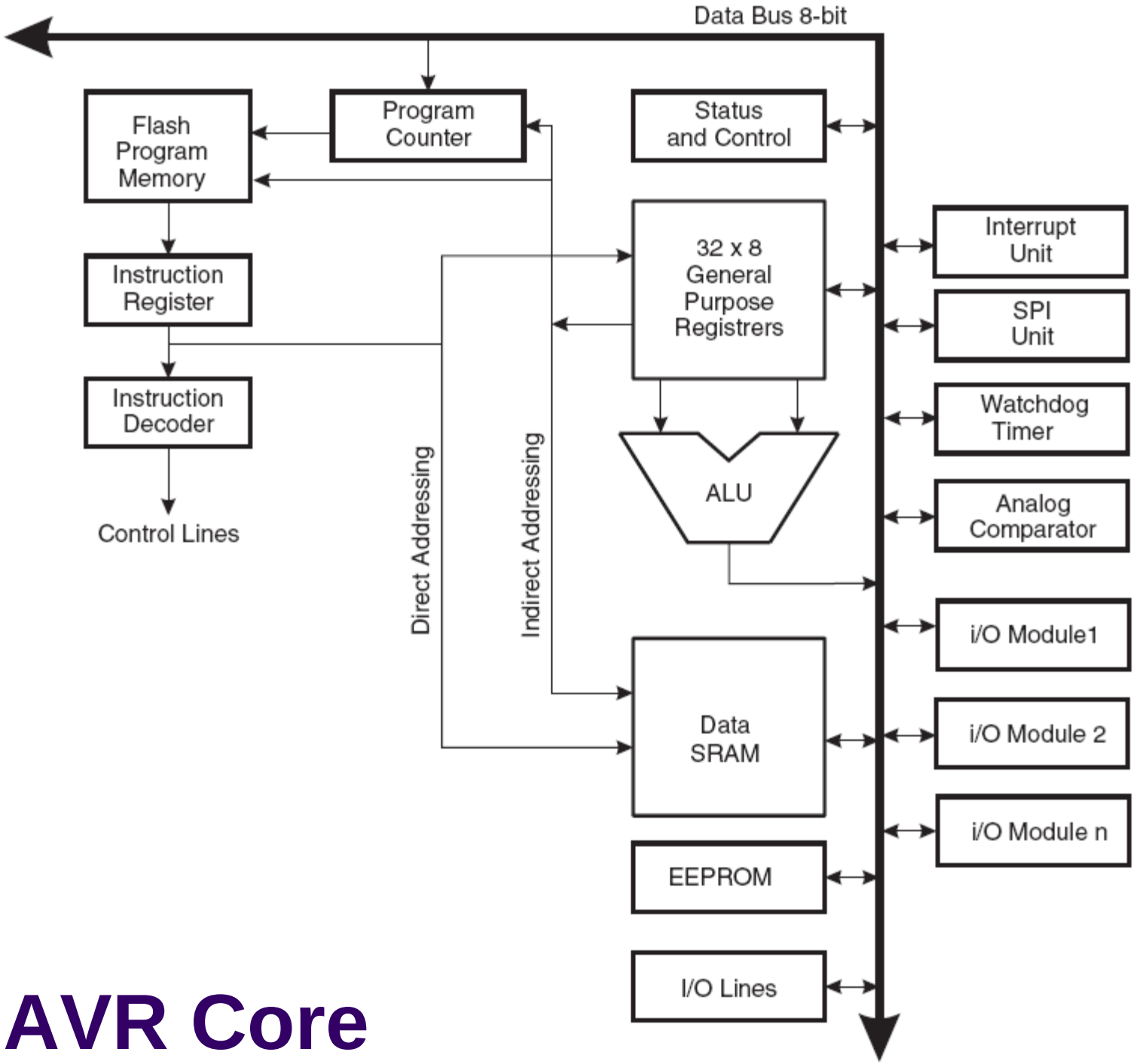
Core

Task 1

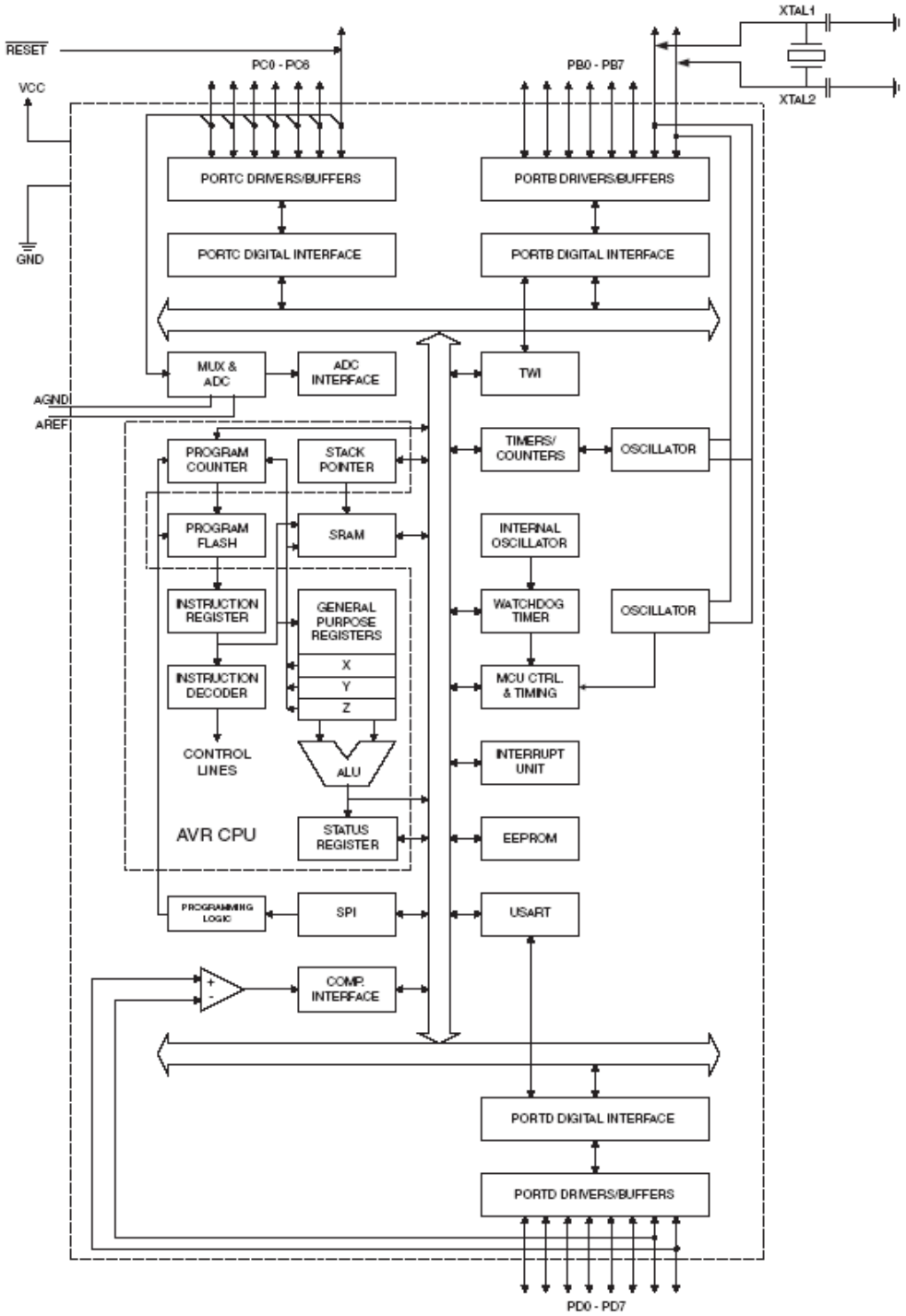
Find and download:

- AVR instruction set manual
- ATmega328PB datasheet
- XPlained-MINI datasheet

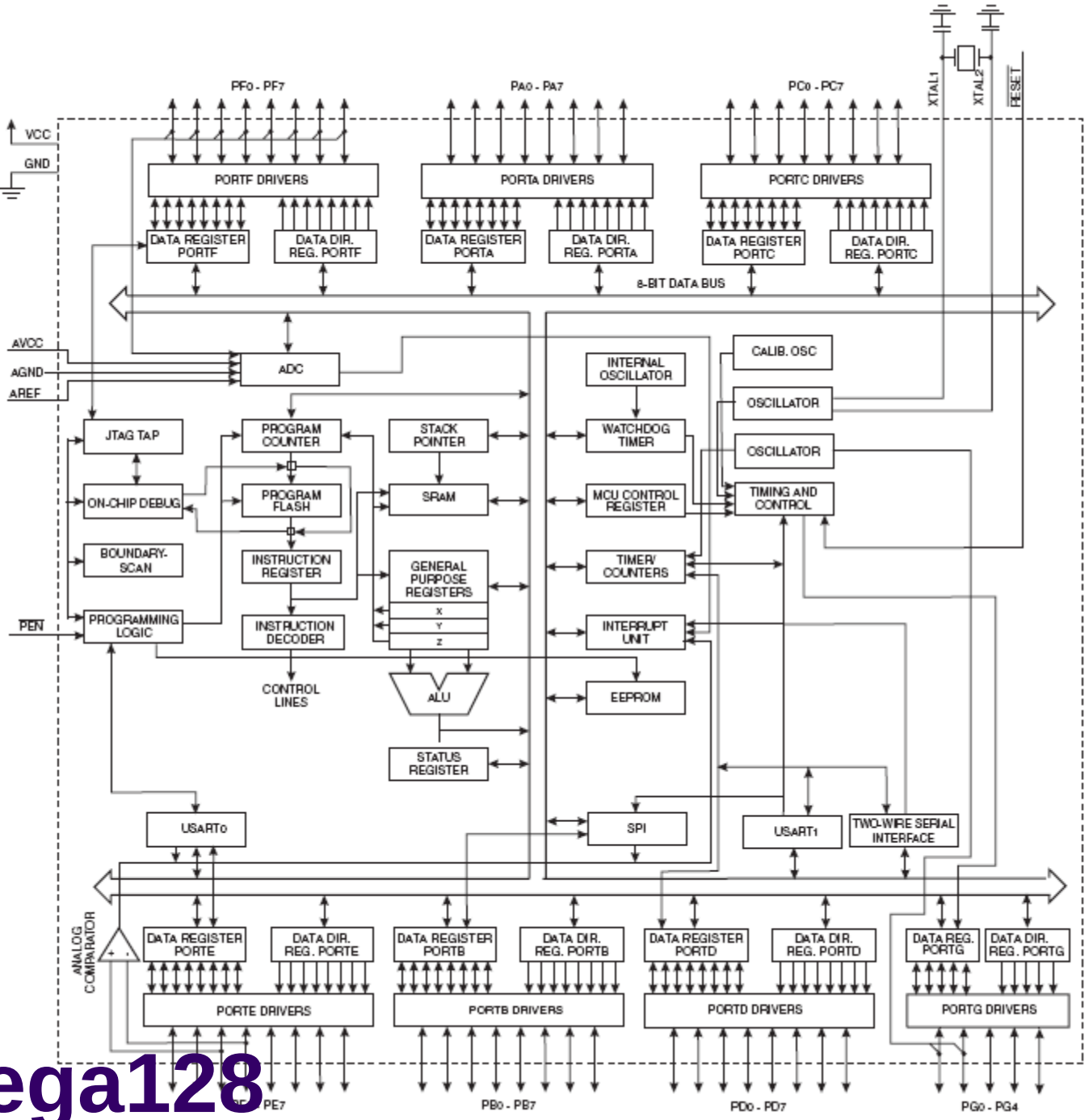
and follow me


Data Bus 8-bit
Flash Program Memory
Program Counter
Status and Control
Instruction Register
Instruction Decoder
Control Lines
32 x 8 General Purpose Registrers
ALU
Direct Addressing
Indirect Addressing
Data SRAM
EEPROM
I/O Lines
Interrupt Unit
SPI Unit
Watchdog Timer
Analog Comparator
i/O Module1
i/O Module 2
i/O Module n

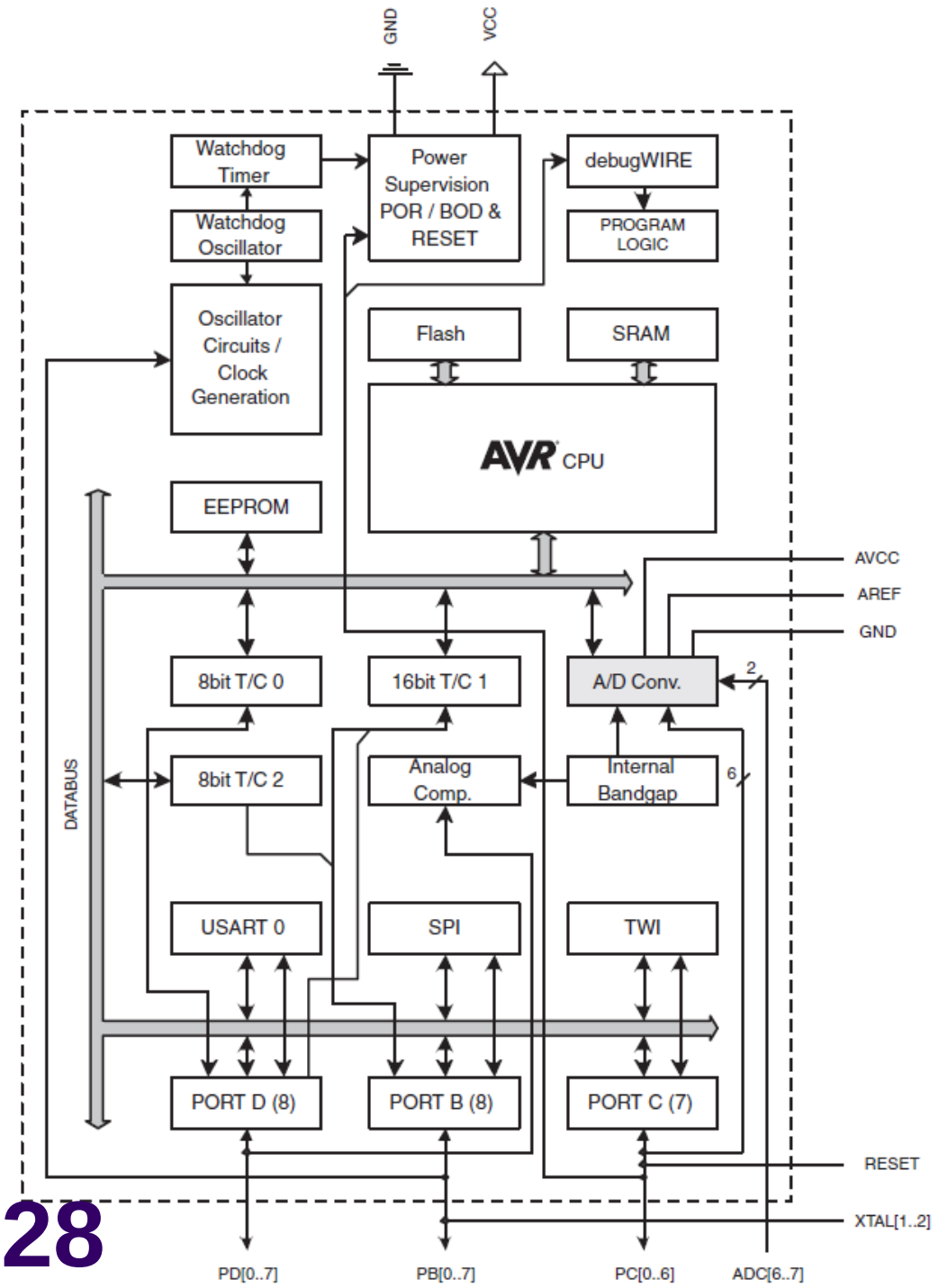
AVR Core


RESET
VCC
GND
PC0 - PC6
PB0 - PB7
XTAL1
XTAL2
PORTC DRIVERS/BUFFERS
PORTB DRIVERS/BUFFERS
PORTC DIGITAL INTERFACE
PORTB DIGITAL INTERFACE
MUX & ADC
ADC INTERFACE
TWI
AGND
AREF
PROGRAM COUNTER
STACK POINTER
TIMERS/ COUNTERS
OSCILLATOR
PROGRAM FLASH
SRAM
INTERNAL OSCILLATOR
INSTRUCTION REGISTER
GENERAL PURPOSE REGISTERS
X
Y
Z
WATCHDOG TIMER
OSCILLATOR
INSTRUCTION DECODER
MCU CTRL & TIMING
CONTROL LINES
ALU
INTERRUPT UNIT
AVR CPU
STATUS REGISTER
EEPROM
PROGRAMMING LOGIC
SPI
USART
COMP. INTERFACE
PORTD DIGITAL INTERFACE
PORTD DRIVERS/BUFFERS
PD0 - PD7

ATmega8


PF0 - PF7
PA0 - PA7
PC0 - PC7
XTAL1
XTAL2
RESET
VCC
GND
PORTF DRIVERS
PORTA DRIVERS
PORTC DRIVERS
DATA REGISTER PORTF
DATA DIR. REG. PORTF
DATA REGISTER PORTA
DATA DIR. REG. PORTA
DATA REGISTER PORTC
DATA DIR. REG. PORTC
8-BIT DATA BUS
AVCC
AGND
AREF
ADC
INTERNAL OSCILLATOR
CALIB. OSC
OSCILLATOR
OSCILLATOR
TIMING AND CONTROL
JTAG TAP
PROGRAM COUNTER
STACK POINTER
WATCHDOG TIMER
ON-CHIP DEBUG
PROGRAM FLASH
SRAM
MCU CONTROL REGISTER
BOUNDARY-SCAN
INSTRUCTION REGISTER
GENERAL PURPOSE REGISTERS
X
Y
Z
TIMER/ COUNTERS
PEN
PROGRAMMING LOGIC
INSTRUCTION DECODER
INTERRUPT UNIT
CONTROL LINES
ALU
EEPROM
STATUS REGISTER
USART0
SPI
USART1
TWO-WIRE SERIAL INTERFACE
ANALOG COMPARATOR
DATA REGISTER PORTE
DATA DIR. REG. PORTE
DATA REGISTER PORTB
DATA DIR. REG. PORTB
DATA REGISTER PORTD
DATA DIR. REG. PORTD
DATA REG. PORTG
DATA DIR. REG. PORTG
PORTE DRIVERS
PORTB DRIVERS
PORTD DRIVERS
PORTG DRIVERS
PE7
PB0 - PB7
PD0 - PD7
PG0 - PG4

ATmega128


GND
VCC
Watchdog Timer
Watchdog Oscillator
Power Supervision POR / BOD & RESET
debugWIRE
PROGRAM LOGIC
Oscillator Circuits / Clock Generation
Flash
SRAM
AVR CPU
EEPROM
AVCC
AREF
GND
8bit T/C 0
16bit T/C 1
A/D Conv.
2
DATABUS
8bit T/C 2
Analog Comp.
Internal Bandgap
6
USART 0
SPI
TWI
PORT D (8)
PORT B (8)
PORT C (7)
RESET
XTAL[1..2]
PD[0..7]
PB[0..7]
PC[0..6]
ADC[6..7]

ATmega328

Memories

- In-system reprogrammable Flash Program Memory
- SRAM Data Memory
- EEPROM Data Memory

Memory Model

- 3 address spaces
  - Program Flash
  - Register File + Data SRAM + I/O
  - EEPROM

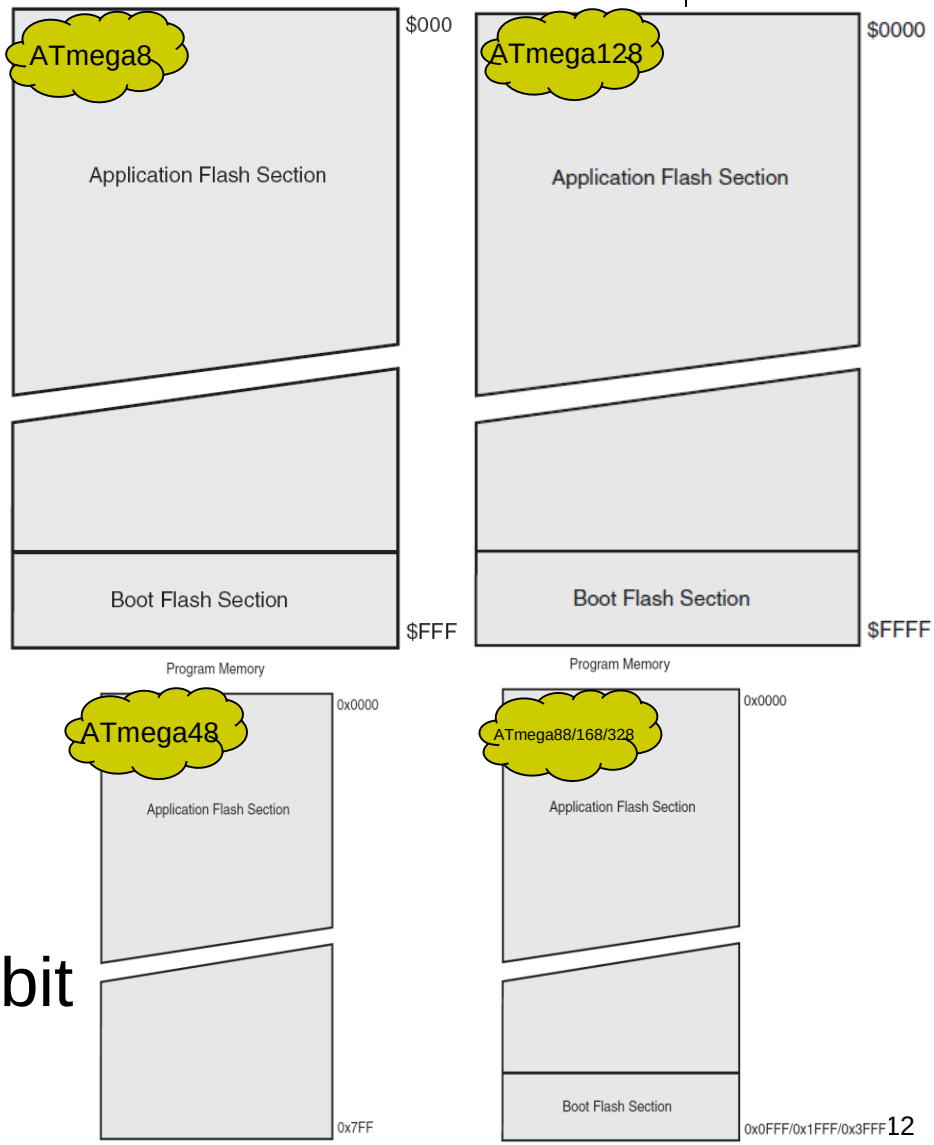
Memory – Program flash

- Instructions 16/32 bits
- ATmega8:
  - Program Counter 12bit

  ⇨ memory 4K x 16bit
- ATmega128:
  - Program Counter 16bit

  ⇨ memory 64K x 16bit
- ATmega168/328:
  - Program Counter 13/14bit

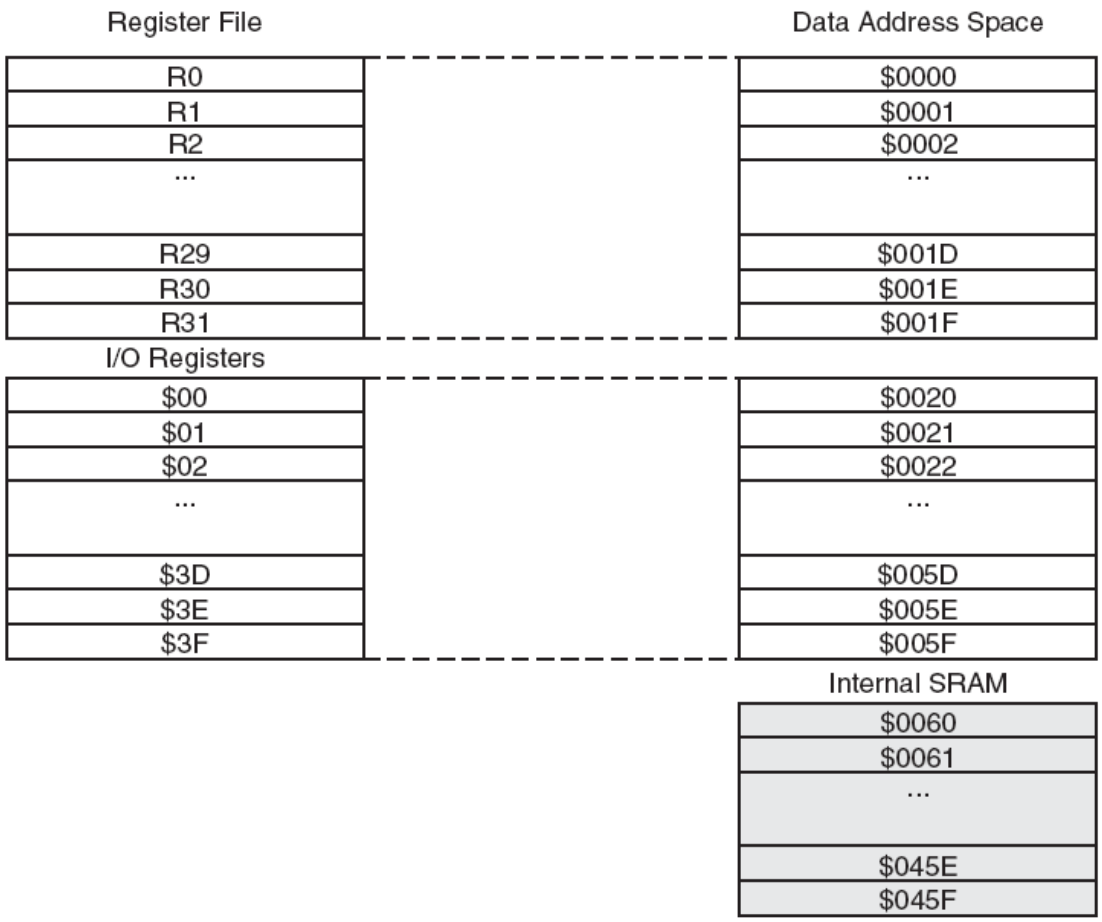
  ⇨ memory 8/16K x 16bit



Memory – SRAM

- Direct
- Indirect
- Indirect with Displacement
- Indirect with Pre-decrement
- Indirect with Post-increment

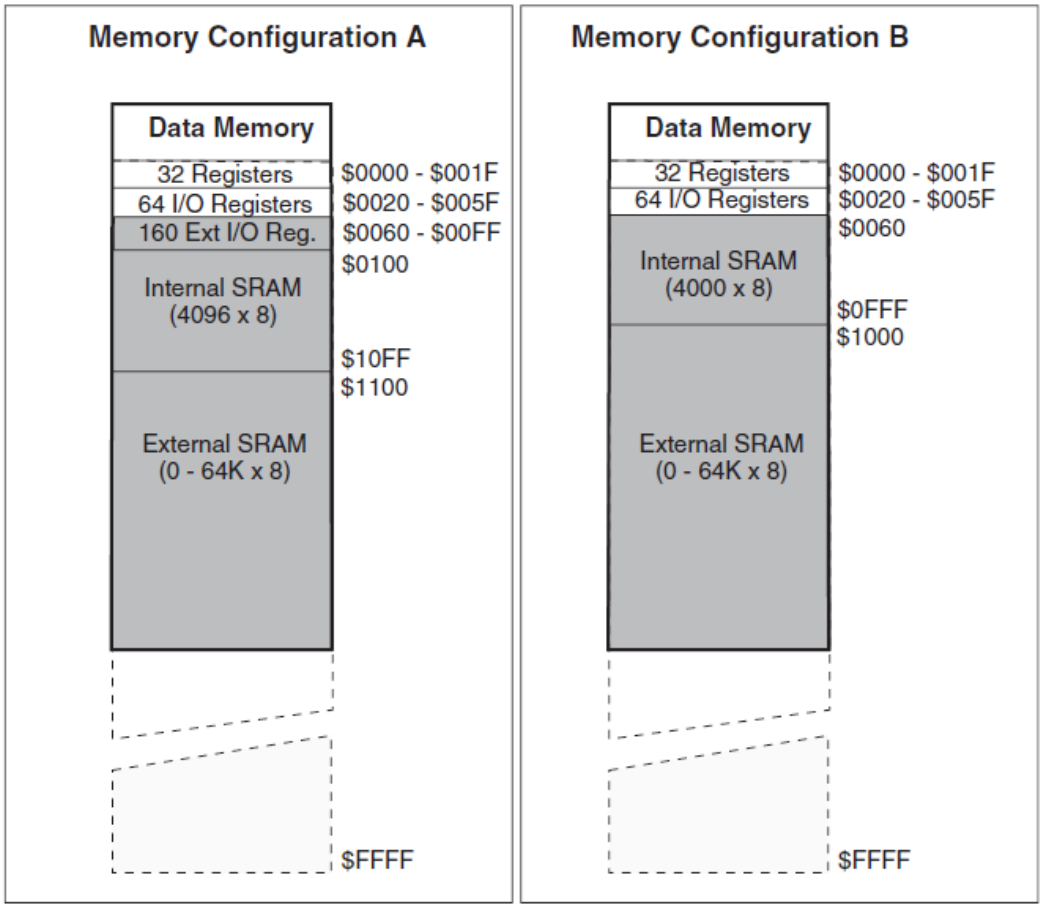
ATmega8:



Memory – SRAM

- Direct
- Indirect
- Indirect with Displacement
- Indirect with Pre-decrement
- Indirect with Post-increment

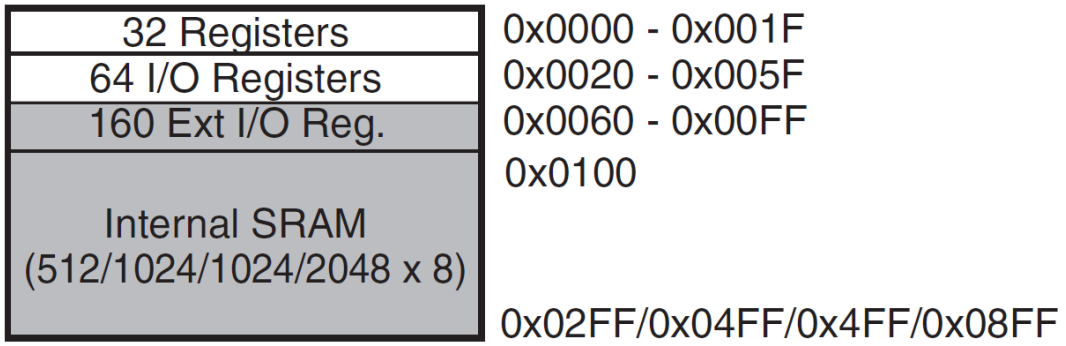
ATmega128:



Memory – SRAM

- Direct
- Indirect
- Indirect with Displacement
- Indirect with Pre-decrement
- Indirect with Post-increment

ATmega88/168/328:



Memory – EEPROM

- ATmega8: 512B
- ATmega128: 4kB
- ATmega168: 512B
- ATmega328: 1kB
- Accessed as other peripherals
  - EEARH/L, EEDR, EECR
  - longer access time (write 8.5ms, read 4 clock cycles)

I/O Space

- control and access to all peripherals
- IN, OUT – transfer between GPR and I/O registers
- ATmega8: 64 x 8bit
- ATmega128:

Register Summary

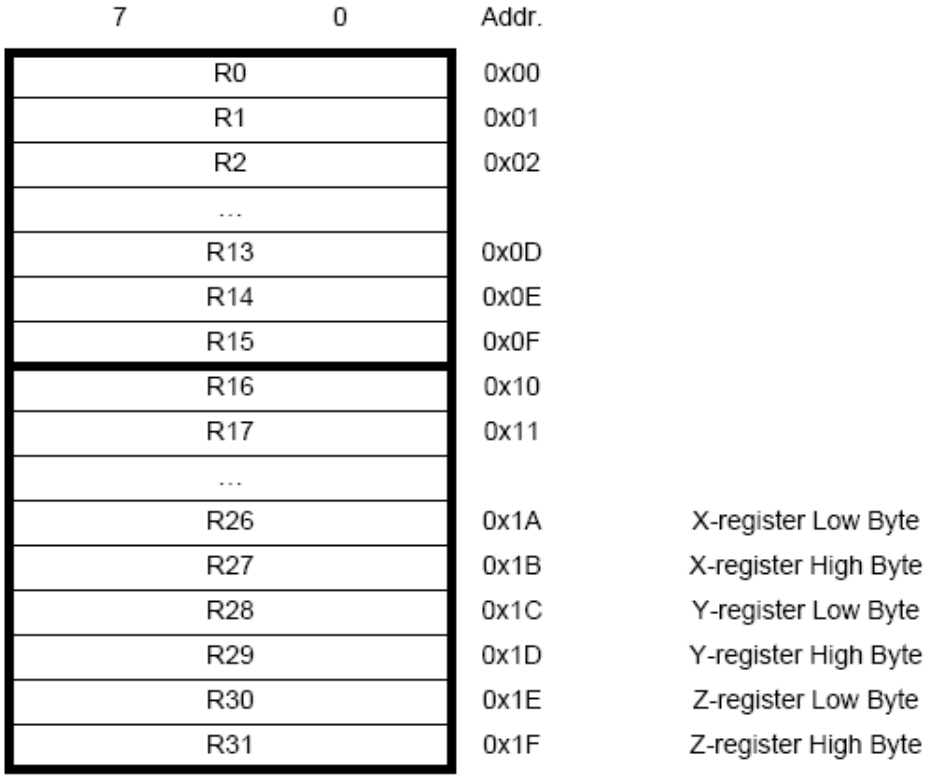
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x3F (0x5F)	SREG	I	T	H	S	V	N	Z	C	9
0x3E (0x5E)	SPH	–	–	–	–	–	SP10	SP9	SP8	11
0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	11
0x3C (0x5C)	Reserved									
0x3B (0x5B)	GICR	INT1	INT0	–	–	–	–	IVSEL	IVCE	47, 65
0x3A (0x5A)	GIFR	INTF1	INTF0	–	–	–	–	–	–	66
0x39 (0x59)	TIMSK	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	–	TOIE0	70, 100, 120
0x38 (0x58)	TIFR	OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	–	TOV0	71, 101, 120
0x37 (0x57)	SPMCR	SPMIE	RWWSB	–	RWWSRE	BLBSET	PGWRT	PGERS	SPMEN	210
0x36 (0x56)	TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	–	TWIE	168
0x35 (0x55)	MCUCR	SE	SM2	SM1	SM0	ISC11	ISC10	ISC01	ISC00	31, 64
0x34 (0x54)	MCUCSR	–	–	–	–	WDRF	BORF	EXTRF	PORF	39
0x33 (0x53)	TCCR0	–	–	–	–	–	CS02	CS01	CS00	70
0x32 (0x52)	TCNT0	Timer/Counter0 (8 Bits)								70
0x31 (0x51)	OSCCAL	Oscillator Calibration Register								29
0x30 (0x50)	SFIOR	–	–	–	–	ACME	PUD	PSR2	PSR10	56, 73, 121, 190
0x2F (0x4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	FOC1A	FOC1B	WGM11	WGM10	95
0x2E (0x4E)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	98
0x2D (0x4D)	TCNT1H	Timer/Counter1 – Counter Register High byte								99
0x2C (0x4C)	TCNT1L	Timer/Counter1 – Counter Register Low byte								99
0x2B (0x4B)	OCR1AH	Timer/Counter1 – Output Compare Register A High byte								99
0x2A (0x4A)	OCR1AL	Timer/Counter1 – Output Compare Register A Low byte								99
0x29 (0x49)	OCR1BH	Timer/Counter1 – Output Compare Register B High byte								99
0x28 (0x48)	OCR1BL	Timer/Counter1 – Output Compare Register B Low byte								99
0x27 (0x47)	ICR1H	Timer/Counter1 – Input Capture Register High byte								100
0x26 (0x46)	ICR1L	Timer/Counter1 – Input Capture Register Low byte								100
0x25 (0x45)	TCCR2	FOC2	WGM20	COM21	COM20	WGM21	CS22	CS21	CS20	115
0x24 (0x44)	TCNT2	Timer/Counter2 (8 Bits)								117
0x23 (0x43)	OCR2	Timer/Counter2 Output Compare Register								117
0x22 (0x42)	ASSR	–	–	–	–	AS2	TCN2UB	OCR2UB	TCR2UB	117
0x21 (0x41)	WDTCR	–	–	–	WDCE	WDE	WDP2	WDP1	WDP0	41
0x20[1] (0x40)[2]	UBRRH	URSEL	–	–	–	UBRR[11:8]				155
	UCSRC	URSEL	UMSEL	UPM1	UPM0	USBS	UCSZ1	UCSZ0	UCPOL	153
0x1F (0x3F)	EEARH	–	–	–	–	–	–	–	EEAR8	18
0x1E (0x3E)	EEARL	EEAR7	EEAR6	EEAR5	EEAR4	EEAR3	EEAR2	EEAR1	EEAR0	18
0x1D (0x3D)	EEDR	EEPROM Data Register								18
0x1C (0x3C)	EECR	–	–	–	–	EERIE	EEMWE	EEWE	EERE	18
0x1B (0x3B)	Reserved									
0x1A (0x3A)	Reserved									
0x19 (0x39)	Reserved									
0x18 (0x38)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	63
0x17 (0x37)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	63
0x16 (0x36)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	63
0x15 (0x35)	PORTC	–	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	63
0x14 (0x34)	DDRC	–	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	63
0x13 (0x33)	PINC	–	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	63
0x12 (0x32)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	63
0x11 (0x31)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	63
0x10 (0x30)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	63
0x0F (0x2F)	SPDR	SPI Data Register								128
0x0E (0x2E)	SPSR	SPIF	WCOL	–	–	–	–	–	SPI2X	128
0x0D (0x2D)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	126
0x0C (0x2C)	UDR	USART I/O Data Register								150
0x0B (0x2B)	UCSRA	RXC	TXC	UDRE	FE	DOR	PE	U2X	MPCM	151
0x0A (0x2A)	UCSRB	RXCIE	TXCIE	UDRIE	RXEN	TXEN	UCSZ2	RXB8	TXB8	152
0x09 (0x29)	UBRRL	USART Baud Rate Register Low byte								155
0x08 (0x28)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	191
0x07 (0x27)	ADMUX	REFS1	REFS0	ADLAR	–	MUX3	MUX2	MUX1	MUX0	202
0x06 (0x26)	ADCSRA	ADEN	ADSC	ADFR	ADIF	ADIE	ADPS2	ADPS1	ADPS0	204
0x05 (0x25)	ADCH	ADC Data Register High byte								205
0x04 (0x24)	ADCL	ADC Data Register Low byte								205
0x03 (0x23)	TWDR	Two-wire Serial Interface Data Register								170
0x02 (0x22)	TWAR	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE	170
0x01 (0x21)	TWSR	TWS7	TWS6	TWS5	TWS4	TWS3	–	TWPS1	TWPS0	170
0x00 (0x20)	TWBR	Two-wire Serial Interface Bit Rate Register								168

GPRF General Purpose Register File

32 x 8bit

Combinations:

- 1x8 out 1x8 in
- 2x8 out 1x8 in
- 2x8 out 1x16 in
- 1x16 out 1x16 in



X,Y,Z: displacement, increment, decrement

MCU Control and Status Register

MCUCSR

7	6	5	4	3	2	1	0
JTD	-	-	JTRF	WDRF	BORF	EXTRF	PORF
R/W	R	R	R/W	R/W	R/W	R/W	R/W
0	0	0					

JTD JTAG Interface Disable (not on 48/88/168/328)

JTRF JTAG Reset Flag (not on 48/88/168/328)

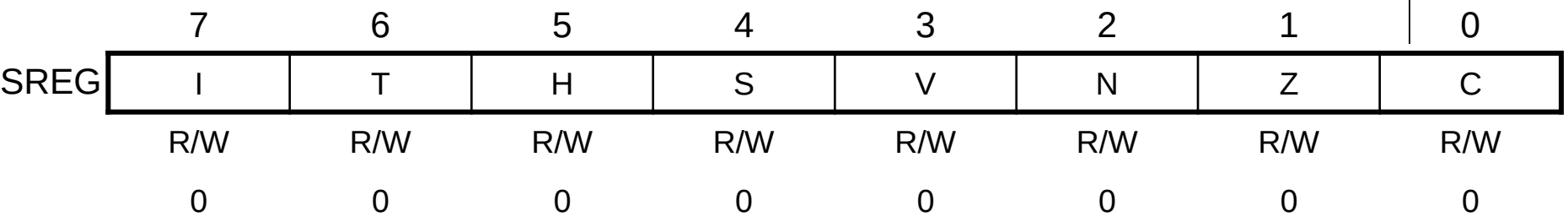
WDRF Watchdog Reset Flag

BORF Brown-out Reset Flag

EXTRF External Reset Flag

PORF Power-on Reset Flag

ALU – Status Register



	7	6	5	4	3	2	1	0
SREG	I	T	H	S	V	N	Z	C
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	0	0	0	0	0	0	0	0

I Global Interrupt Enable

T Bit Copy Storage

H Half-Carry

S Sign

V Two’s Complement Overflow

N Negative

Z Zero

C Carry

Stack – ATmega8/128 and many others

	7	6	5	4	3	2	1	0
SPH	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8
SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0

Stack – ATmega48/88/168/328

	7	6	5	4	3	2	1	0
SPH	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8
SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	RAMEND	RAMEND	RAMEND	RAMEND	RAMEND	RAMEND	RAMEND	RAMEND
	RAMEND	RAMEND	RAMEND	RAMEND	RAMEND	RAMEND	RAMEND	RAMEND

ATmega8: 0x00(0x20) – 0x3F(0x5F)

27. Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x3F (0x5F)	SREG	I	T	H	S	V	N	Z	C	8
0x3E (0x5E)	SPH	–	–	–	–	–	SP10	SP9	SP8	11
0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	11
0x3C (0x5C)	Reserved									
0x3B (0x5B)	GICR	INT1	INT0	–	–	–	–	IVSEL	IVCE	48, 68
0x3A (0x5A)	GIFR	INTF1	INTF0	–	–	–	–	–	–	69
0x39 (0x59)	TIMSK	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	–	TOIE0	73, 104, 124
0x38 (0x58)	TIFR	OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	–	TOV0	74, 104, 104
0x37 (0x57)	SPMCR	SPMIE	RWWSB	–	RWWSRE	BLBSET	PGWRT	PGERS	SPMEN	224
0x36 (0x56)	TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	–	TWIE	191
0x35 (0x55)	MCUCR	SE	SM2	SM1	SM0	ISC11	ISC10	ISC01	ISC00	36, 67
0x34 (0x54)	MCUCSR	–	–	–	–	WDRF	BORF	EXTRF	PORF	43
0x33 (0x53)	TCCR0	–	–	–	–	–	CS02	CS01	CS00	73
0x32 (0x52)	TCNT0	Timer/Counter0 (8 Bits)								73
0x31 (0x51)	OSCCAL	Oscillator Calibration Register								31
0x30 (0x50)	SFIOR	–	–	–	–	ACME	PUD	PSR2	PSR10	57, 77, 125, 196
0x2F (0x4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	FOC1A	FOC1B	WGM11	WGM10	99
0x2E (0x4E)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	101
0x2D (0x4D)	TCNT1H	Timer/Counter1 – Counter Register High byte								102
0x2C (0x4C)	TCNT1L	Timer/Counter1 – Counter Register Low byte								102
0x2B (0x4B)	OCR1AH	Timer/Counter1 – Output Compare Register A High byte								103
0x2A (0x4A)	OCR1AL	Timer/Counter1 – Output Compare Register A Low byte								103
0x29 (0x49)	OCR1BH	Timer/Counter1 – Output Compare Register B High byte								103
0x28 (0x48)	OCR1BL	Timer/Counter1 – Output Compare Register B Low byte								103
0x27 (0x47)	ICR1H	Timer/Counter1 – Input Capture Register High byte								103
0x26 (0x46)	ICR1L	Timer/Counter1 – Input Capture Register Low byte								103
0x25 (0x45)	TCCR2	FOC2	WGM20	COM21	COM20	WGM21	CS22	CS21	CS20	121
0x24 (0x44)	TCNT2	Timer/Counter2 (8 Bits)								123
0x23 (0x43)	OCR2	Timer/Counter2 Output Compare Register								123
0x22 (0x42)	ASSR	–	–	–	–	AS2	TCN2UB	OCR2UB	TCR2UB	123
0x21 (0x41)	WDTCR	–	–	–	WDCE	WDE	WDP2	WDP1	WDP0	43
0x20[1] (0x40)[1]	UBRRH	URSEL	–	–	–	UBRR[11:8]				160
	UCSRC	URSEL	UMSEL	UPM1	UPM0	USBS	UCSZ1	UCSZ0	UCPOL	159
0x1F (0x3F)	EEARH	–	–	–	–	–	–	–	EEAR8	19
0x1E (0x3E)	EEARL	EEAR7	EEAR6	EEAR5	EEAR4	EEAR3	EEAR2	EEAR1	EEAR0	19
0x1D (0x3D)	EEDR	EEPROM Data Register								19
0x1C (0x3C)	EECR	–	–	–	–	EERIE	EEMWE	EEWE	EERE	19
0x1B (0x3B)	Reserved									
0x1A (0x3A)	Reserved									
0x19 (0x39)	Reserved									
0x18 (0x38)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	65
0x17 (0x37)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	65
0x16 (0x36)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	65
0x15 (0x35)	PORTC	–	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	65
0x14 (0x34)	DDRC	–	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	65
0x13 (0x33)	PINC	–	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	65
0x12 (0x32)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	65
0x11 (0x31)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	65
0x10 (0x30)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	66
0x0F (0x2F)	SPDR	SPI Data Register								135
0x0E (0x2E)	SPSR	SPIF	WCOL	–	–	–	–	–	SPI2X	134
0x0D (0x2D)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	133
0x0C (0x2C)	UDR	USART I/O Data Register								156
0x0B (0x2B)	UCSRA	RXC	TXC	UDRE	FE	DOR	PE	U2X	MPCM	157
0x0A (0x2A)	UCSRB	RXCIE	TXCIE	UDRIE	RXEN	TXEN	UCSZ2	RXB8	TXB8	158
0x09 (0x29)	UBRRL	USART Baud Rate Register Low byte								160
0x08 (0x28)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	196
0x07 (0x27)	ADMUX	REFS1	REFS0	ADLAR	–	MUX3	MUX2	MUX1	MUX0	208
0x06 (0x26)	ADCSRA	ADEN	ADSC	ADFR	ADIF	ADIE	ADPS2	ADPS1	ADPS0	209
0x05 (0x25)	ADCH	ADC Data Register High byte								210
0x04 (0x24)	ADCL	ADC Data Register Low byte								210
0x03 (0x23)	TWDR	Two-wire Serial Interface Data Register								193
0x02 (0x22)	TWAR	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE	194
0x01 (0x21)	TWSR	TWS7	TWS6	TWS5	TWS4	TWS3	–	TWPS1	TWPS0	193
0x00 (0x20)	TWBR	Two-wire Serial Interface Bit Rate Register								191

27. Register Summary ATmega8

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x3F (0x5F)	SREG	I	T	H	S	V	N	Z	C	8
0x3E (0x5E)	SPH	–	–	–	–	–	SP10	SP9	SP8	11
0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	11
0x3C (0x5C)	Reserved									
0x3B (0x5B)	GICR	INT1	INT0	–	–	–	–	IVSEL	IVCE	48, 68
0x3A (0x5A)	GIFR	INTF1	INTF0	–	–	–	–	–	–	69
0x39 (0x59)	TIMSK	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	–	TOIE0	73, 104, 124
0x38 (0x58)	TIFR	OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	–	TOV0	74, 104, 104
0x37 (0x57)	SPMCR	SPMIE	RWWSB	–	RWWSRE	BLBSET	PGWRT	PGERS	SPMEN	224
0x36 (0x56)	TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	–	TWIE	191
0x35 (0x55)	MCUCR	SE	SM2	SM1	SM0	ISC11	ISC10	ISC01	ISC00	36, 67
0x34 (0x54)	MCUCSR	–	–	–	–	WDRF	BORF	EXTRF	PORF	43
0x33 (0x53)	TCCR0	–	–	–	–	–	CS02	CS01	CS00	73
0x32 (0x52)	TCNT0	Timer/Counter0 (8 Bits)								73
0x31 (0x51)	OSCCAL	Oscillator Calibration Register								31
0x30 (0x50)	SFIOR	–	–	–	–	ACME	PUD	PSR2	PSR10	57, 77, 125, 196
0x2F (0x4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	FOC1A	FOC1B	WGM11	WGM10	99
0x2E (0x4E)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	101
0x2D (0x4D)	TCNT1H	Timer/Counter1 – Counter Register High byte								102
0x2C (0x4C)	TCNT1L	Timer/Counter1 – Counter Register Low byte								102
0x2B (0x4B)	OCR1AH	Timer/Counter1 – Output Compare Register A High byte								103
0x2A (0x4A)	OCR1AL	Timer/Counter1 – Output Compare Register A Low byte								103
0x29 (0x49)	OCR1BH	Timer/Counter1 – Output Compare Register B High byte								103
0x28 (0x48)	OCR1BL	Timer/Counter1 – Output Compare Register B Low byte								103
0x27 (0x47)	ICR1H	Timer/Counter1 – Input Capture Register High byte								103
0x26 (0x46)	ICR1L	Timer/Counter1 – Input Capture Register Low byte								103
0x25 (0x45)	TCCR2	FOC2	WGM20	COM21	COM20	WGM21	CS22	CS21	CS20	121
0x24 (0x44)	TCNT2	Timer/Counter2 (8 Bits)								123
0x23 (0x43)	OCR2	Timer/Counter2 Output Compare Register								123
0x22 (0x42)	ASSR	–	–	–	–	AS2	TCN2UB	OCR2UB	TCR2UB	123
0x21 (0x41)	WDTCR	–	–	–	WDCE	WDE	WDP2	WDP1	WDP0	43
0x20[1] (0x40)[1]	UBRRH	URSEL	–	–	–	UBRR[11:8]				160
	UCSRC	URSEL	UMSEL	UPM1	UPM0	USBS	UCSZ1	UCSZ0	UCPOL	159
0x1F (0x3F)	EEARH	–	–	–	–	–	–	–	EEAR8	19
0x1E (0x3E)	EEARL	EEAR7	EEAR6	EEAR5	EEAR4	EEAR3	EEAR2	EEAR1	EEAR0	19
0x1D (0x3D)	EEDR	EEPROM Data Register								19
0x1C (0x3C)	EECR	–	–	–	–	EERIE	EEMWE	EEWE	EERE	19
0x1B (0x3B)	Reserved									
0x1A (0x3A)	Reserved									

0x2C (0x4C)	TCNT1L	Timer/Counter1 – Counter Register Low byte								102
0x2B (0x4B)	OCR1AH	Timer/Counter1 – Output Compare Register A High byte								103
0x2A (0x4A)	OCR1AL	Timer/Counter1 – Output Compare Register A Low byte								103
0x29 (0x49)	OCR1BH	Timer/Counter1 – Output Compare Register B High byte								103
0x28 (0x48)	OCR1BL	Timer/Counter1 – Output Compare Register B Low byte								103
0x27 (0x47)	ICR1H	Timer/Counter1 – Input Capture Register High byte								103
0x26 (0x46)	ICR1L	Timer/Counter1 – Input Capture Register Low byte								103
0x25 (0x45)	TCCR2	FOC2	WGM20	COM21	COM20	WGM21	CS22	CS21	CS20	121
0x24 (0x44)	TCNT2	Timer/Counter2 (8 Bits)								123
0x23 (0x43)	OCR2	Timer/Counter2 Output Compare Register								123
0x22 (0x42)	ASSR	–	–	–	–	AS2	TCN2UB	OCR2UB	TCR2UB	123
0x21 (0x41)	WDTCR	–	–	–	WDCE	WDE	WDP2	WDP1	WDP0	43
0x20[1] (0x40)[1]	UBRRH	URSEL	–	–	–	UBRR[11:8]				160
	UCSRC	URSEL	UMSEL	UPM1	UPM0	USBS	UCSZ1	UCSZ0	UCPOL	159
0x1F (0x3F)	EEARH	–	–	–	–	–	–	–	EEAR8	19
0x1E (0x3E)	EEARL	EEAR7	EEAR6	EEAR5	EEAR4	EEAR3	EEAR2	EEAR1	EEAR0	19
0x1D (0x3D)	EEDR	EEPROM Data Register								19
0x1C (0x3C)	EECR	–	–	–	–	EERIE	EEMWE	EEWE	EERE	19
0x1B (0x3B)	Reserved									
0x1A (0x3A)	Reserved									
0x19 (0x39)	Reserved									
0x18 (0x38)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	65
0x17 (0x37)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	65
0x16 (0x36)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	65
0x15 (0x35)	PORTC	–	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	65
0x14 (0x34)	DDRC	–	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	65
0x13 (0x33)	PINC	–	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	65
0x12 (0x32)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	65
0x11 (0x31)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	65
0x10 (0x30)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	66
0x0F (0x2F)	SPDR	SPI Data Register								135
0x0E (0x2E)	SPSR	SPIF	WCOL	–	–	–	–	–	SPI2X	134
0x0D (0x2D)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	133
0x0C (0x2C)	UDR	USART I/O Data Register								156
0x0B (0x2B)	UCSRA	RXC	TXC	UDRE	FE	DOR	PE	U2X	MPCM	157
0x0A (0x2A)	UCSRB	RXCIE	TXCIE	UDRIE	RXEN	TXEN	UCSZ2	RXB8	TXB8	158
0x09 (0x29)	UBRRL	USART Baud Rate Register Low byte								160
0x08 (0x28)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	196
0x07 (0x27)	ADMUX	REFS1	REFS0	ADLAR	–	MUX3	MUX2	MUX1	MUX0	208
0x06 (0x26)	ADCSRA	ADEN	ADSC	ADFR	ADIF	ADIE	ADPS2	ADPS1	ADPS0	209
0x05 (0x25)	ADCH	ADC Data Register High byte								210
0x04 (0x24)	ADCL	ADC Data Register Low byte								210
0x03 (0x23)	TWDR	Two-wire Serial Interface Data Register								193
0x02 (0x22)	TWAR	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE	194
0x01 (0x21)	TWSR	TWS7	TWS6	TWS5	TWS4	TWS3	–	TWPS1	TWPS0	193
0x00 (0x20)	TWBR	Two-wire Serial Interface Bit Rate Register								191

ATmega128: 0x00(0x20) – 0x3F(0x5F) + (0x60)-(0x9D)

Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
($FF)	Reserved	–	–	–	–	–	–	–	–	
..	Reserved	–								
($9E)	Reserved	–								
($9D)	UCSR1C	–								
($9C)	UDR1									
($9B)	UCSR1A	RXC1								
($9A)	UCSR1B	RXCIE1								
($99)	UBRR1L									
($98)	UBRR1H	–								
($97)	Reserved	–								
($96)	Reserved	–								
($95)	UCSR0C	–								
($94)	Reserved	–								
($93)	Reserved	–								
($92)	Reserved	–								
($91)	Reserved	–								
($90)	UBRR0H	–								
($8F)	Reserved	–								
($8E)	Reserved	–								
($8D)	Reserved	–								
($8C)	TCCR3C	FOC3A								
($8B)	TCCR3A	COM3A1								
($8A)	TCCR3B	ICNC3								
($89)	TCNT3H									
($88)	TCNT3L									
($87)	OCR3AH									
($86)	OCR3AL									
($85)	OCR3BH									
($84)	OCR3BL									
($83)	OCR3CH									
($82)	OCR3CL									
($81)	ICR3H									
($80)	ICR3L									
($7F)	Reserved	–								
($7E)	Reserved	–								
($7D)	ETIMSK	–								
($7C)	ETIFR	–								
($7B)	Reserved	–								
($7A)	TCCR1C	FOC1A								
($79)	OCR1CH									
($78)	OCR1CL									
($77)	Reserved	–								
($76)	Reserved	–								
($75)	Reserved	–								
($74)	TWCR	TWINT								
($73)	TWDR									
($72)	TWAR	TWA6								
($71)	TWSR	TWS7								
($70)	TWBR									
($6F)	OSCCAL									
($6E)	Reserved	–								
($6D)	XMCRA	–								
($6C)	XMCRB	XMBK								
($6B)	Reserved	–								
($6A)	EICRA	ISC31								
($69)	Reserved	–								
($68)	SPMCSR	SPMIE								
($67)	Reserved	–								
($66)	Reserved	–								
($65)	PORTG	–								
($64)	DDRG	–								
($63)	PING	–								
($62)	PORTF	PORTF7								

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
($61)	DDRF	DDF7	DDF6	DDF5	DDF4	DDF3	DDF2	DDF1	DDF0	88
($60)	Reserved	–	–	–	–	–	–	–	–	
$3F ($5F)	SREG	I	T	H	S	V	N	Z	C	10
$3E ($5E)	SPH	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	13
$3D ($5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	13
$3C ($5C)	XDIV	XDIVEN	XDIV6	XDIV5	XDIV4	XDIV3	XDIV2	XDIV1	XDIV0	36
$3B ($5B)	RAMPZ	–	–	–	–	–	–	–	RAMPZ0	13
$3A ($5A)	EICRB	ISC71	ISC70	ISC61	ISC60	ISC51	ISC50	ISC41	ISC40	90
$39 ($59)	EIMSK	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0	91
$38 ($58)	EIFR	INTF7	INTF6	INTF5	INTF4	INTF3	INTF	INTF1	INTF0	91
$37 ($57)	TIMSK	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	OCIE0	TOIE0	108, 138, 158
$36 ($56)	TIFR	OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	OCF0	TOV0	108, 140, 159
$35 ($55)	MCUCR	SRE	SRW10	SE	SM1	SM0	SM2	IVSEL	IVCE	30, 44, 63
$34 ($54)	MCUCSR	JTD	–	–	JTRF	WDRF	BORF	EXTRF	PORF	53, 254
$33 ($53)	TCCR0	FOC0	WGM00	COM01	COM00	WGM01	CS02	CS01	CS00	103
$32 ($52)	TCNT0	Timer/Counter0 (8 Bit)								105
$31 ($51)	OCR0	Timer/Counter0 Output Compare Register								105
$30 ($50)	ASSR	–	–	–	–	AS0	TCN0UB	OCR0UB	TCR0UB	106
$2F ($4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	COM1C1	COM1C0	WGM11	WGM10	132
$2E ($4E)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	135
$2D ($4D)	TCNT1H	Timer/Counter1 – Counter Register High Byte								137
$2C ($4C)	TCNT1L	Timer/Counter1 – Counter Register Low Byte								137
$2B ($4B)	OCR1AH	Timer/Counter1 – Output Compare Register A High Byte								137
$2A ($4A)	OCR1AL	Timer/Counter1 – Output Compare Register A Low Byte								137
$29 ($49)	OCR1BH	Timer/Counter1 – Output Compare Register B High Byte								137
$28 ($48)	OCR1BL	Timer/Counter1 – Output Compare Register B Low Byte								137
$27 ($47)	ICR1H	Timer/Counter1 – Input Capture Register High Byte								138
$26 ($46)	ICR1L	Timer/Counter1 – Input Capture Register Low Byte								138
$25 ($45)	TCCR2	FOC2	WGM20	COM21	COM20	WGM21	CS22	CS21	CS20	156
$24 ($44)	TCNT2	Timer/Counter2 (8 Bit)								158
$23 ($43)	OCR2	Timer/Counter2 Output Compare Register								158
$22 ($42)	OCDR	IDRD/OCDR7	OCDR6	OCDR5	OCDR4	OCDR3	OCDR2	OCDR1	OCDR0	251
$21 ($41)	WDTCR	–	–	–	WDCE	WDE	WDP2	WDP1	WDP0	55
$20 ($40)	SFIOR	TSM	–	–	–	ACME	PUD	PSR0	PSR321	72, 109, 144, 227
$1F ($3F)	EEARH	–	–	–	–	EEPROM Address Register High				20
$1E ($3E)	EEARL	EEPROM Address Register Low Byte								20
$1D ($3D)	EEDR	EEPROM Data Register								21
$1C ($3C)	EECR	–	–	–	–	EERIE	EEMWE	EEWE	EERE	21
$1B ($3B)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	86
$1A ($3A)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	86
$19 ($39)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	86
$18 ($38)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	86
$17 ($37)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	86
$16 ($36)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	86
$15 ($35)	PORTC	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	86
$14 ($34)	DDRC	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	86
$13 ($33)	PINC	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	87
$12 ($32)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	87
$11 ($31)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	87
$10 ($30)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	87
$0F ($2F)	SPDR	SPI Data Register								168
$0E ($2E)	SPSR	SPIF	WCOL	–	–	–	–	–	SPI2X	168
$0D ($2D)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	166
$0C ($2C)	UDR0	USART0 I/O Data Register								188
$0B ($2B)	UCSR0A	RXC0	TXC0	UDRE0	FE0	DOR0	UPE0	U2X0	MPCM0	188
$0A ($2A)	UCSR0B	RXCIE0	TXCIE0	UDRIE0	RXEN0	TXEN0	UCSZ02	RXB80	TXB80	189
$09 ($29)	UBRR0L	USART0 Baud Rate Register Low								191
$08 ($28)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	227
$07 ($27)	ADMUX	REFS1	REFS0	ADLAR	MUX4	MUX3	MUX2	MUX1	MUX0	242
$06 ($26)	ADCSRA	ADEN	ADSC	ADFR	ADIF	ADIE	ADPS2	ADPS1	ADPS0	244
$05 ($25)	ADCH	ADC Data Register High Byte								245
$04 ($24)	ADCL	ADC Data Register Low Byte								245
$03 ($23)	PORTE	PO								
$02 ($22)	DDRE	DD								

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
$01 ($21)	PINE	PINE7	PINE6	PINE5	PINE4	PINE3	PINE2	PINE1	PINE0	87
$00 ($20)	PINF	PINF7	PINF6	PINF5	PINF4	PINF3	PINF2	PINF1	PINF0	88

Register Summary ATmega128

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
($FF)	Reserved	–	–	–	–	–	–	–	–	
..	Reserved	–	–	–	–	–	–	–	–	
($9E)	Reserved	–	–	–	–	–	–	–	–	
($9D)	UCSR1C	–	UMSEL1	UPM11	UPM10	USBS1	UCSZ11	UCSZ10	UCPOL1	190
($9C)	UDR1	USART1 I/O Data Register								188
($9B)	UCSR1A	RXC1	TXC1	UDRE1	FE1	DOR1	UPE1	U2X1	MPCM1	188
($9A)	UCSR1B	RXCIE1	TXCIE1	UDRIE1	RXEN1	TXEN1	UCSZ12	RXB81	TXB81	189
($99)	UBRR1L	USART1 Baud Rate Register Low								191
($98)	UBRR1H	–	–	–	–	USART1 Baud Rate Register High				191
($97)	Reserved	–	–	–	–	–	–	–	–	
($96)	Reserved	–	–	–	–	–	–	–	–	
($95)	UCSR0C	–	UMSEL0	UPM01	UPM00	USBS0	UCSZ01	UCSZ00	UCPOL0	190
($94)	Reserved	–	–	–	–	–	–	–	–	
($93)	Reserved	–	–	–	–	–	–	–	–	
($92)	Reserved	–	–	–	–	–	–	–	–	
($91)	Reserved	–	–	–	–	–	–	–	–	
($90)	UBRR0H	–	–	–	–	USART0 Baud Rate Register High				191
($8F)	Reserved	–	–	–	–	–	–	–	–	
($8E)	Reserved	–	–	–	–	–	–	–	–	
($8D)	Reserved	–	–	–	–	–	–	–	–	
($8C)	TCCR3C	FOC3A	FOC3B	FOC3C	–	–	–	–	–	136
($8B)	TCCR3A	COM3A1	COM3A0	COM3B1	COM3B0	COM3C1	COM3C0	WGM31	WGM30	132
($8A)	TCCR3B	ICNC3	ICES3	–	WGM33	WGM32	CS32	CS31	CS30	135
($89)	TCNT3H	Timer/Counter3 – Counter Register High Byte								137
($88)	TCNT3L	Timer/Counter3 – Counter Register Low Byte								137
($87)	OCR3AH	Timer/Counter3 – Output Compare Register A High Byte								137
($86)	OCR3AL	Timer/Counter3 – Output Compare Register A Low Byte								137
($85)	OCR3BH	Timer/Counter3 – Output Compare Register B High Byte								138
($84)	OCR3BL	Timer/Counter3 – Output Compare Register B Low Byte								138
($83)	OCR3CH	Timer/Counter3 – Output Compare Register C High Byte								138
($82)	OCR3CL	Timer/Counter3 – Output Compare Register C Low Byte								138
($81)	ICR3H	Timer/Counter3 – Input Capture Register High Byte								138
($80)	ICR3L	Timer/Counter3 – Input Capture Register Low Byte								138
($7F)	Reserved	–	–	–	–	–	–	–	–	
($7E)	Reserved	–	–	–	–	–	–	–	–	
($7D)	ETIMSK	–	–	TICIE3	OCIE3A	OCIE3B	TOIE3	OCIE3C	OCIE1C	139
($7C)	ETIFR	–	–	ICF3	OCF3A	OCF3B	TOV3	OCF3C	OCF1C	140
($7B)	Reserved	–	–	–	–	–	–	–	–	
($7A)	TCCR1C	FOC1A	FOC1B	FOC1C	–	–	–	–	–	136

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
($61)	DDRF	DDF7	DDF6	DDF5	DDF4	DDF3	DDF2	DDF1	DDF0	88
($60)	Reserved	–	–	–	–	–	–	–	–	
$3F ($5F)	SREG	I	T	H	S	V	N	Z	C	10
$3E ($5E)	SPH	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	13
$3D ($5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	13
$3C ($5C)	XDIV	XDIVEN	XDIV6	XDIV5	XDIV4	XDIV3	XDIV2	XDIV1	XDIV0	36
$3B ($5B)	RAMPZ	–	–	–	–	–	–	–	RAMPZ0	13
$3A ($5A)	EICRB	ISC71	ISC70	ISC61	ISC60	ISC51	ISC50	ISC41	ISC40	90
$39 ($59)	EIMSK	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0	91
$38 ($58)	EIFR	INTF7	INTF6	INTF5	INTF4	INTF3	INTF	INTF1	INTF0	91
$37 ($57)	TIMSK	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	OCIE0	TOIE0	108, 138, 158
$36 ($56)	TIFR	OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	OCF0	TOV0	108, 140, 159
$35 ($55)	MCUCR	SRE	SRW10	SE	SM1	SM0	SM2	IVSEL	IVCE	30, 44, 63
$34 ($54)	MCUCSR	JTD	–	–	JTRF	WDRF	BORF	EXTRF	PORF	53, 254
$33 ($53)	TCCR0	FOC0	WGM00	COM01	COM00	WGM01	CS02	CS01	CS00	103
$32 ($52)	TCNT0	Timer/Counter0 (8 Bit)								105
$31 ($51)	OCR0	Timer/Counter0 Output Compare Register								105
$30 ($50)	ASSR	–	–	–	–	AS0	TCN0UB	OCR0UB	TCR0UB	106
$2F ($4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	COM1C1	COM1C0	WGM11	WGM10	132
$2E ($4E)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	135
$2D ($4D)	TCNT1H	Timer/Counter1 – Counter Register High Byte								137
$2C ($4C)	TCNT1L	Timer/Counter1 – Counter Register Low Byte								137
$2B ($4B)	OCR1AH	Timer/Counter1 – Output Compare Register A High Byte								137
$2A ($4A)	OCR1AL	Timer/Counter1 – Output Compare Register A Low Byte								137
$29 ($49)	OCR1BH	Timer/Counter1 – Output Compare Register B High Byte								137
$28 ($48)	OCR1BL	Timer/Counter1 – Output Compare Register B Low Byte								137
$27 ($47)	ICR1H	Timer/Counter1 – Input Capture Register High Byte								138
$26 ($46)	ICR1L	Timer/Counter1 – Input Capture Register Low Byte								138
$25 ($45)	TCCR2	FOC2	WGM20	COM21	COM20	WGM21	CS22	CS21	CS20	156
$24 ($44)	TCNT2	Timer/Counter2 (8 Bit)								158
$23 ($43)	OCR2	Timer/Counter2 Output Compare Register								158
$22 ($42)	OCDR	IDRD/OCDR7	OCDR6	OCDR5	OCDR4	OCDR3	OCDR2	OCDR1	OCDR0	251
$21 ($41)	WDTCR	–	–	–	WDCE	WDE	WDP2	WDP1	WDP0	55
$20 ($40)	SFIOR	TSM	–	–	–	ACME	PUD	PSR0	PSR321	72, 109, 144, 227
$1F ($3F)	EEARH	–	–	–	–	EEPROM Address Register High				20
$1E ($3E)	EEARL	EEPROM Address Register Low Byte								20
$1D ($3D)	EEDR	EEPROM Data Register								21
$1C ($3C)	EECR	–	–	–	–	EERIE	EEMWE	EEWE	EERE	21
$1B ($3B)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	86
$1A ($3A)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	86
$19 ($39)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	86

Exceptions to keep you awake

For technical reasons*, I/O register access differs

- Bit operations for some GPIO and communication
- In/out for the most common registers
- All memory access

* 16/32 bit instruction coding

I/O Register Access

- IN/OUT
  - only registers $00-3F (PINF-SREG)

	Syntax:	Operands:
(i)	IN Rd,A	$0 \le d \le 31, 0 \le A \le 63$

16-bit Opcode:

1011	0AAd	dddd	AAAA

I/O Register Access

- CBI/SBI, SBIC/SBIS
  - only registers $00-$1F (PINF-EEARH)

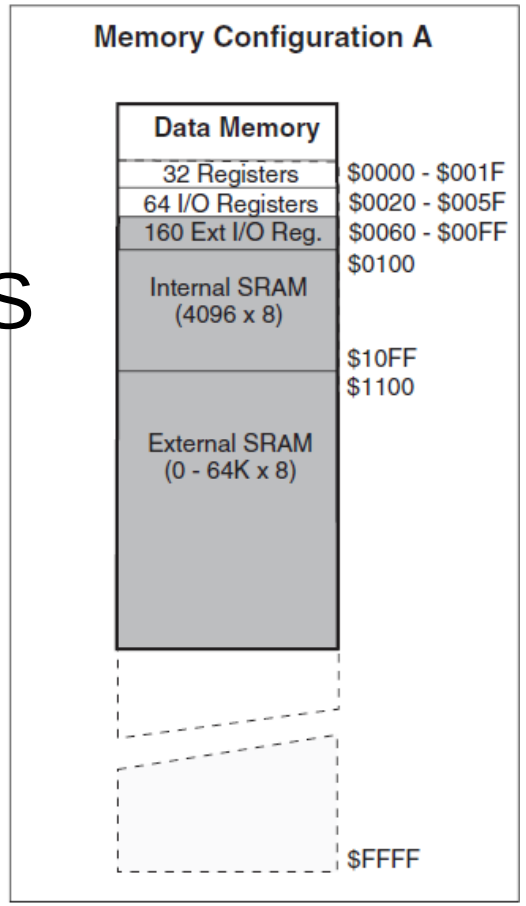
	Syntax:	**Operands:**
(i)	CBI A,b	$0 \leq A \leq 31, 0 \leq b \leq 7$

16-bit Opcode:

1001	1000	AAAA	Abbb

I/O Register Access

- LD/ST, LDD/STD, LDS/STS
  - Whole data space
    - Register File
    - I/O memory
    - internal SRAM
    - external SRAM



Syntax:

(i) LDS Rd,k $0 \le d \le 31, 0 \le k \le 65535$

32-bit Opcode:

1001	000d	dddd	0000
kkkk	kkkk	kkkk	kkkk

Beware

```
CBI MCUCR, SE
```

- CBI operates only $00-$1F, MCUCR is $35 ($55)

```
IN  r16, PORTG
```

- IN operates only I/O space $00-$3F,
  PORTG is in Extended I/O space ($65)

```
LDS r0, OSCCAL
```

- LDS loads only r16-r31

```
LDS r20, PORTD   ≠   IN r20, PORTD
LDS r20, TCNT0   =   IN r20, PORTD
```

- LDS operates the whole Data space,
  IN operates I/O space *with different addresses*

m128def.inc: .equ PORTD = 0x12

$13 ($33)	PINC		$33 ($53)	TCCR0	
$12 ($32)	PORTD		$32 ($52)	TCNT0	
$11 ($31)	DDRD		$31 ($51)	OCR0	