Instructions

8-bit AVR

WARNING – Device specific

Machine instructions

- Simple action
- Perfectly defined effects
- Optimized selection

- At AVR:
- 1 or 2 words (2 or 4 bytes)
  - because of arguments needed
- 1 to 5 cycles
  - arguments, possible prefetch drop, possible stack$_2$op.

(SPM is special)

Addressing modes

- Direct
  - Direct register, single register
  - Direct register, two registers
  - I/O direct
  - Data direct
  - Direct program
- Relative
  - Relative program

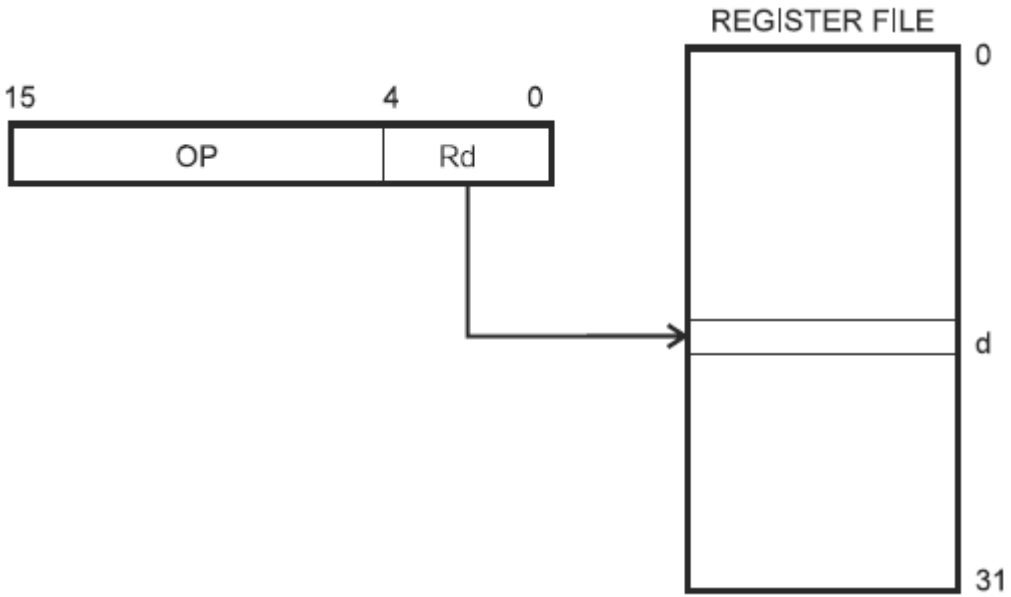
Addressing modes

- Indirect
  - Data indirect
  - Indirect program
- Indirect^{++}
  - Data indirect with displacement
  - Data indirect with pre-decrement
  - Data indirect with post-increment

Operands

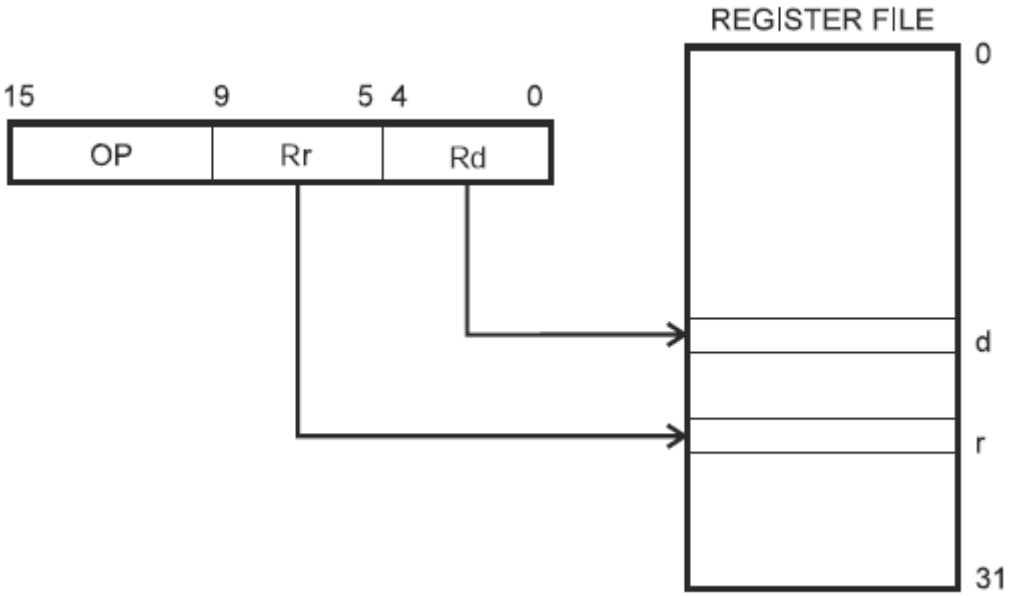
Rd	Destination (and source) register in the Register File
Rr	Source register in the Register File
R	Result after instruction is executed
K	Constant data
k	Constant address
b	Bit in the Register File or I/O Register (3-bit)
s	Bit in the Status Register (3-bit)
X,Y,Z	Indirect Address Register (X=R27:R26, Y=R29:R28, Z=R31:R30)
A	I/O location address
q	Displacement for direct addressing (6-bit)

Register Direct, single register



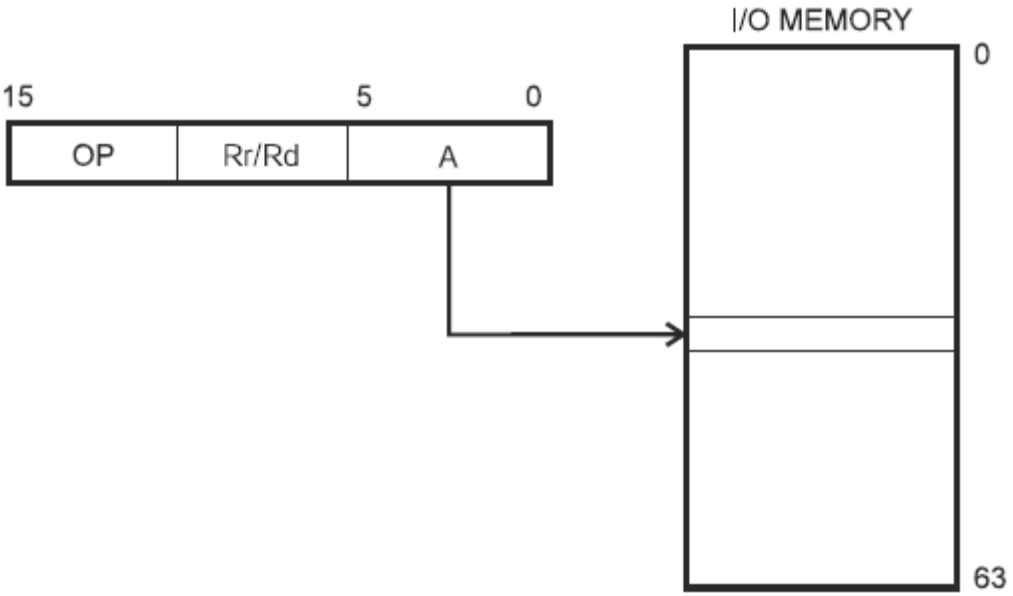
COM NEG INC DEC TST CLR SER PUSH POP LSL LSR ROL ROR ASR SWAP

Register Direct, two registers



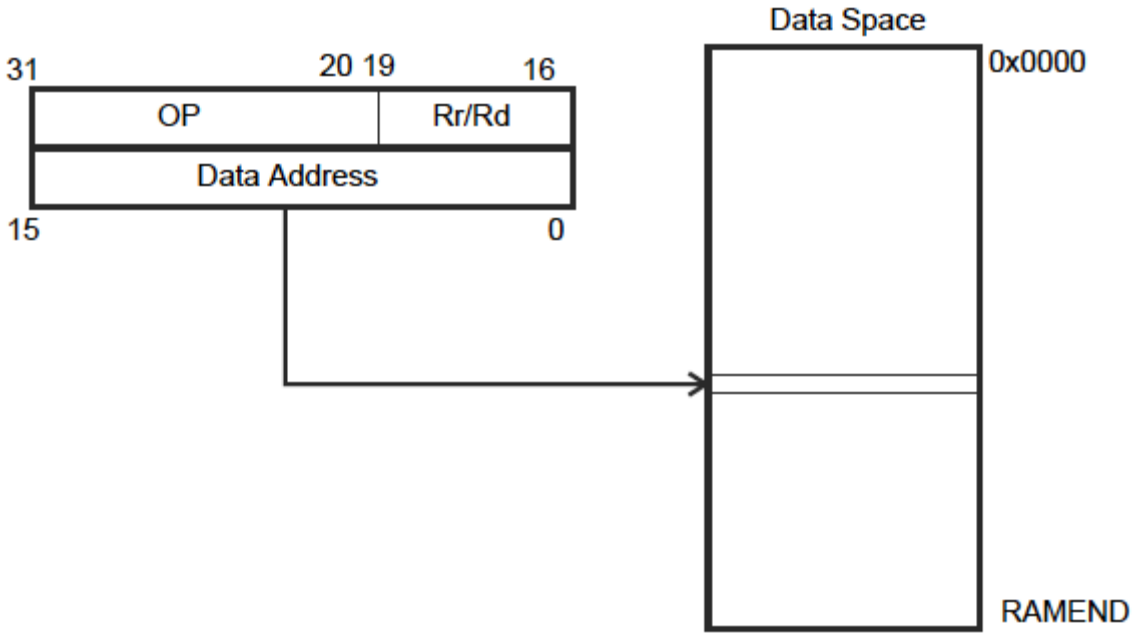
ADD ADC SUB SBC AND OR EOR MUL MULS MULSU FMUL FMULS FMULSU CPSE CP CPC MOV MOVW

I/O Direct



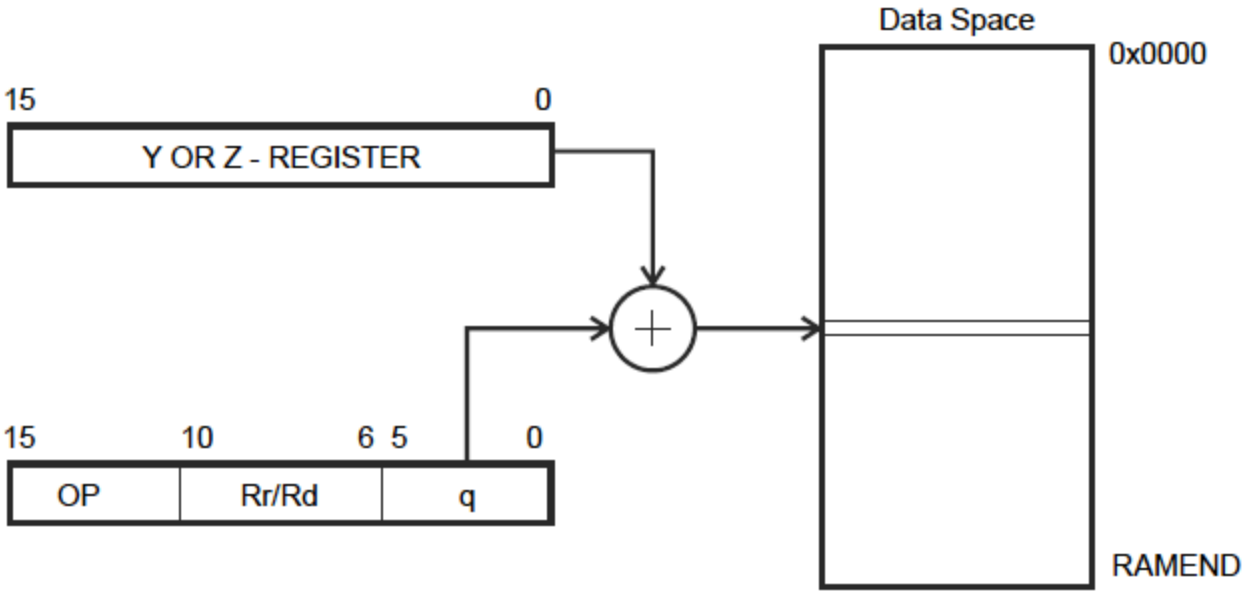
IN OUT

Data Direct



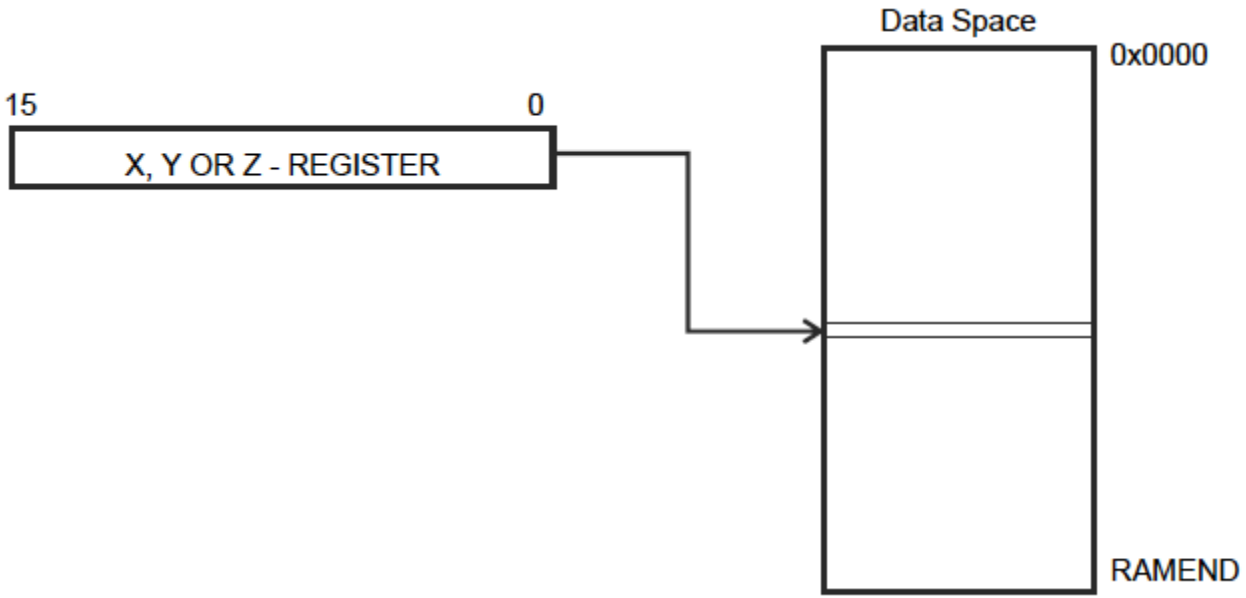
LDS STS

Data Indirect with Displacement

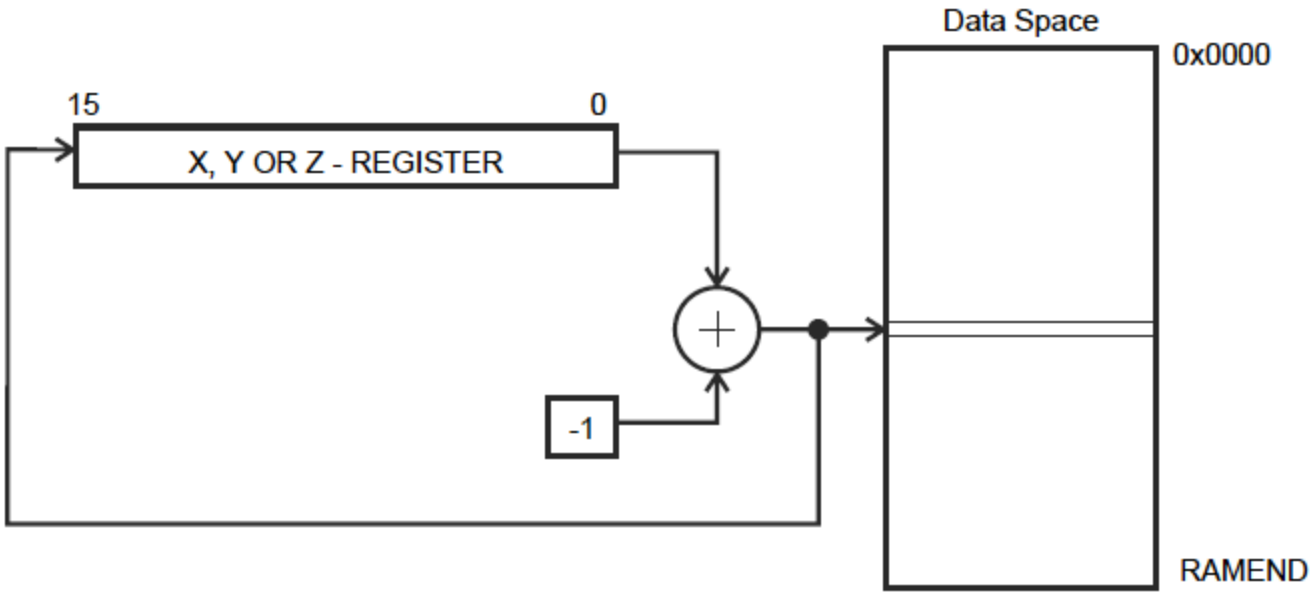


LDD STD

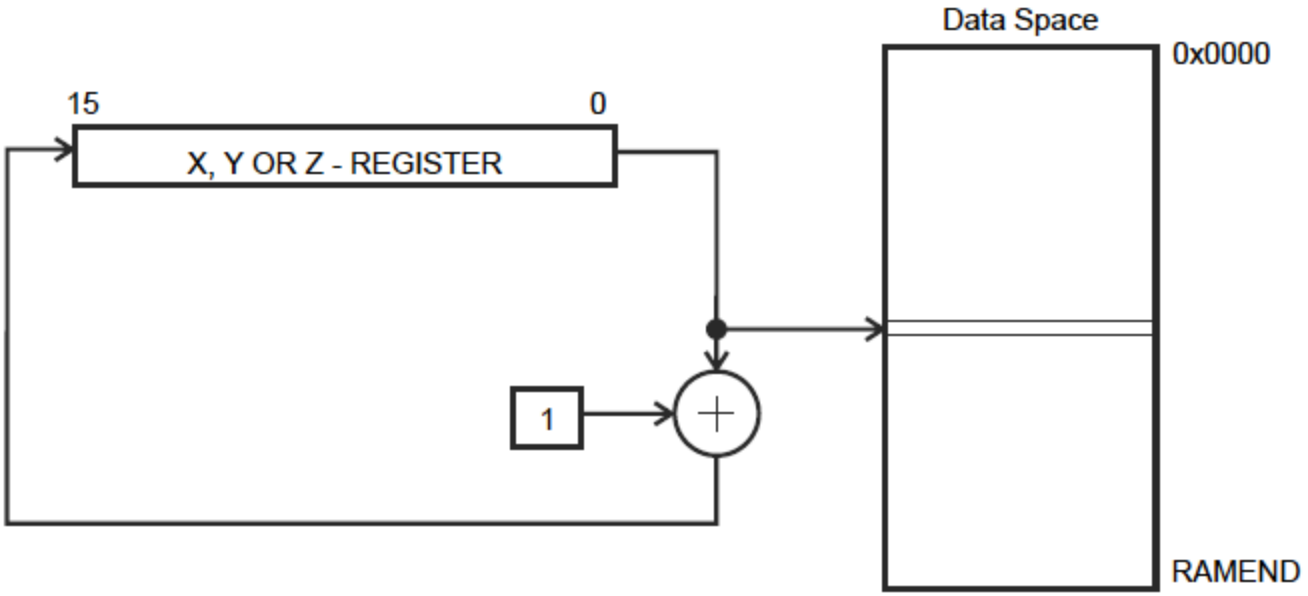
Data Indirect



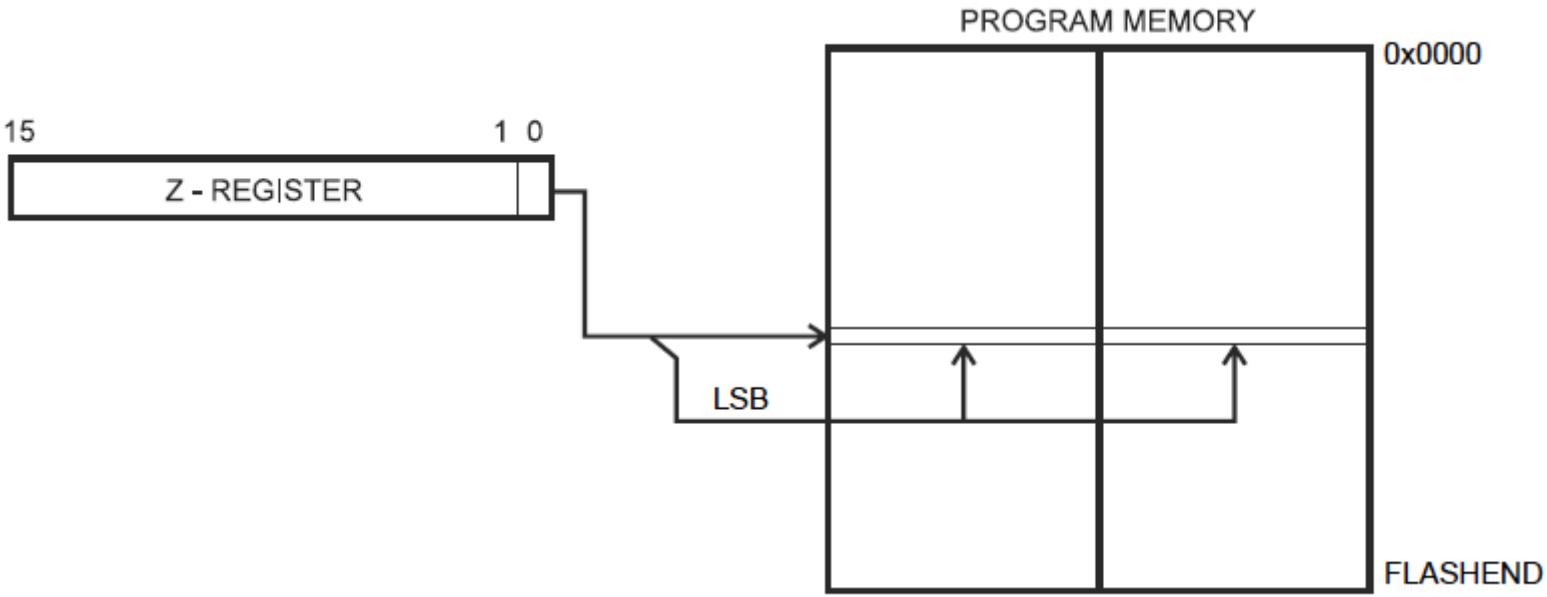
Data Indirect with Pre-decrement



Data Indirect with Post-increment

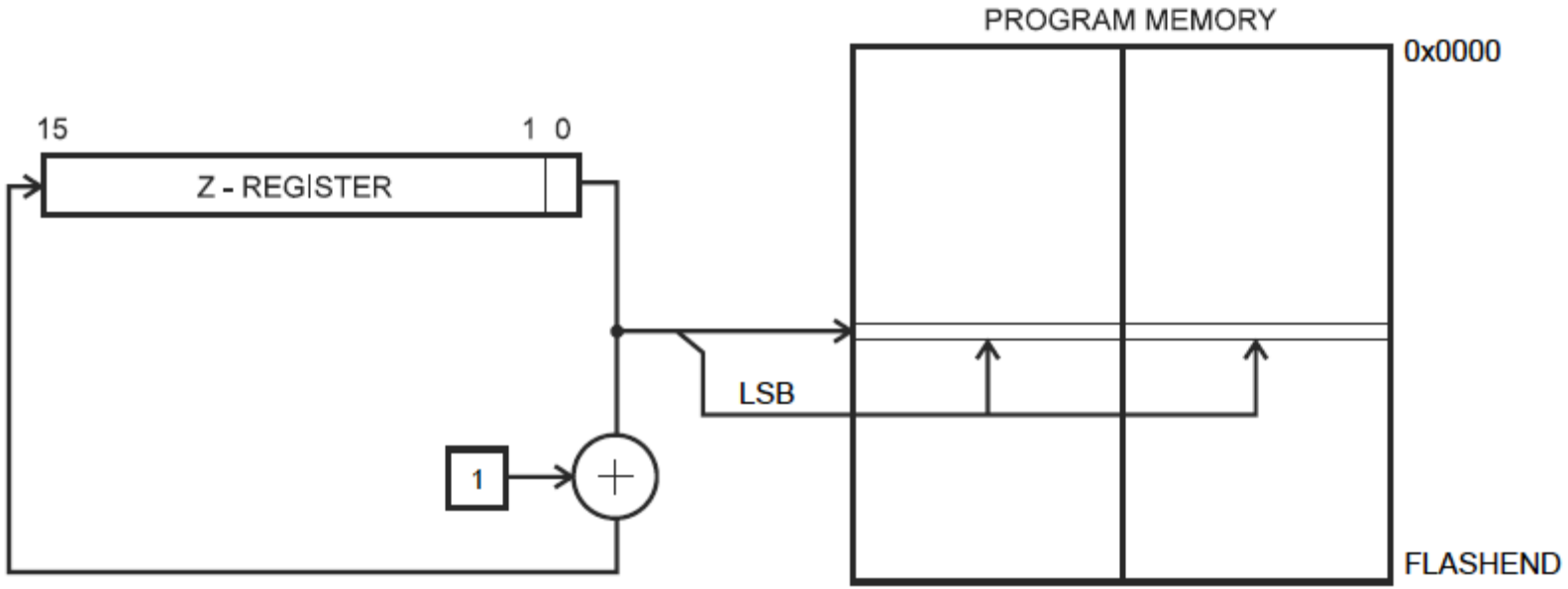


Program Memory Constant



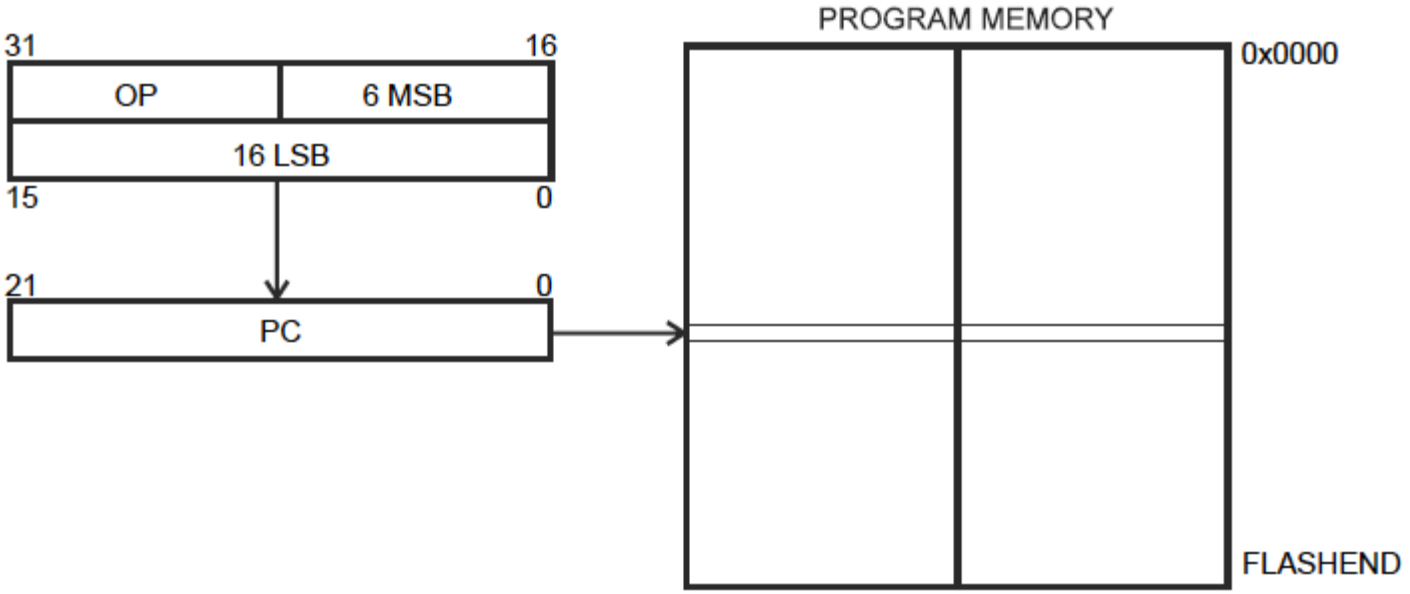
LPM ELPM SPM

Program Memory with Post-increment



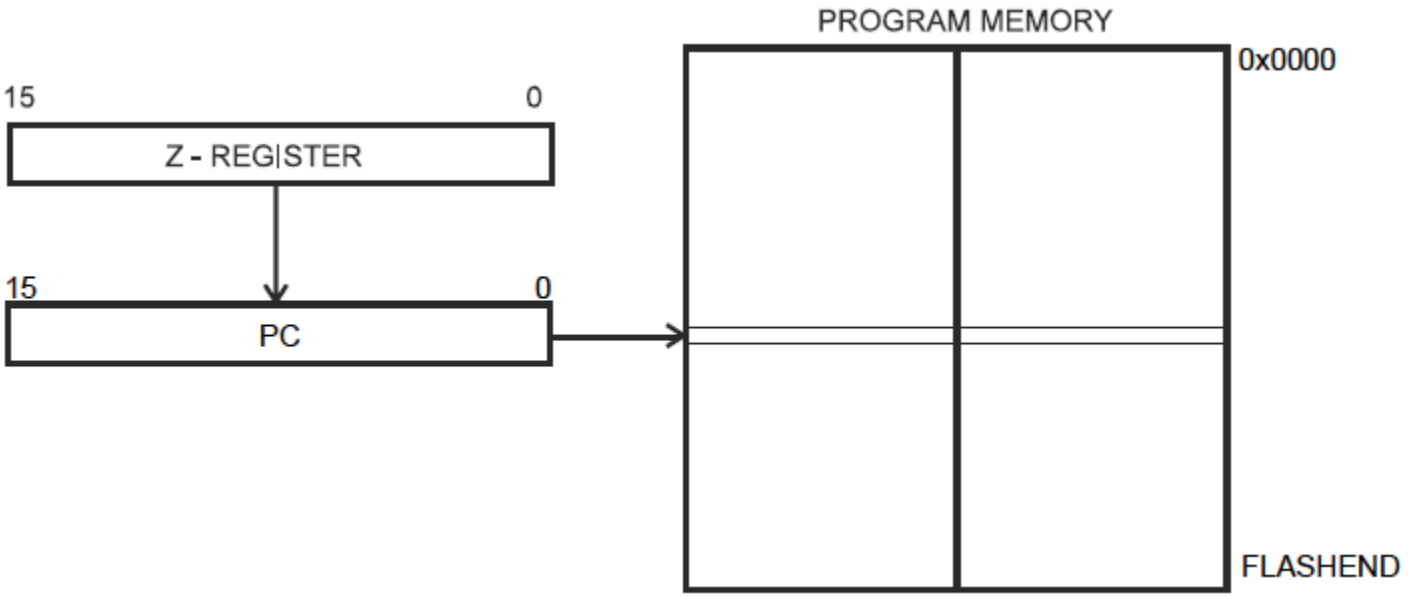
LPM Z+ ELPM Z+

Direct Program



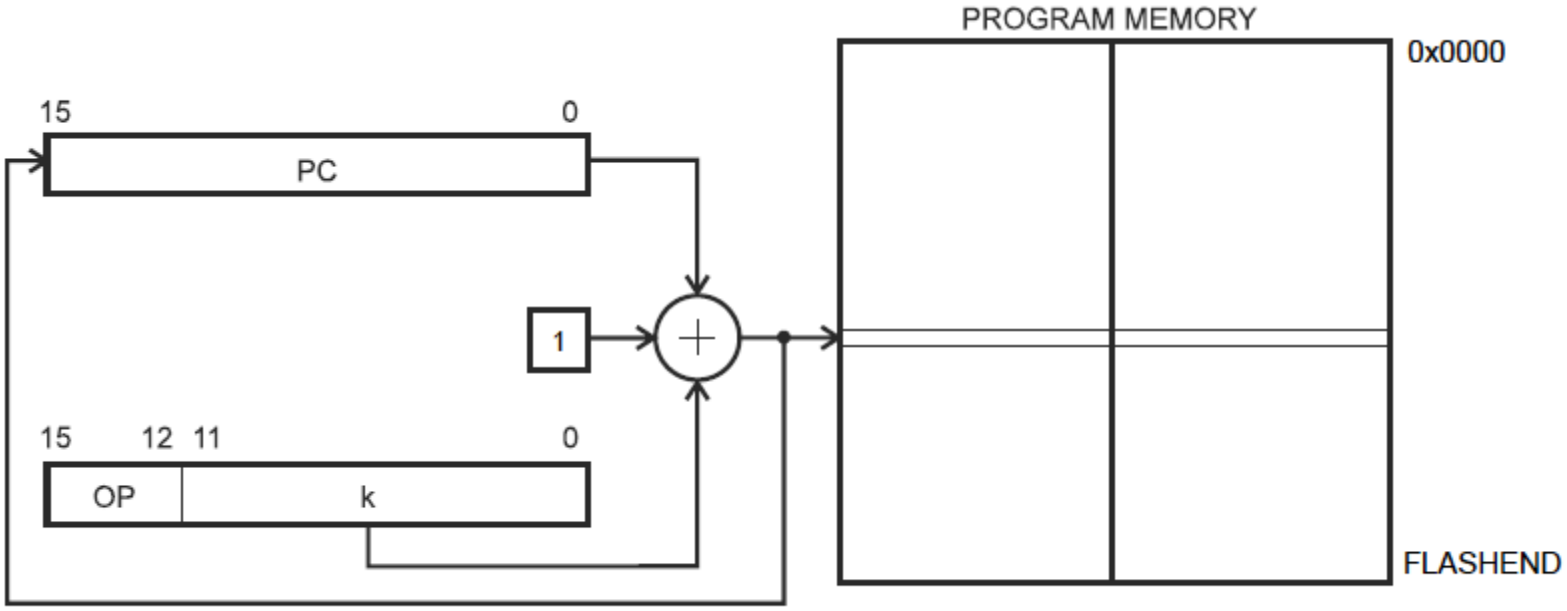
JMP CALL

Indirect Program



IJMP ICALL

Relative Program



RJMP RCALL

Instructions

- Arithmetic and Logic
- Data Transfer
- Bit and Bit-test
- Branch
- MCU Control

Arithmetic and Logic

- ADD SUB SUBI
- ADC SBC SBCI
- ADIW SBIW
- INC DEC TST

- AND ANDI
- OR ORI
- EOR

- COM NEG
- SBR CBR
- SER CLR

- MUL MULS MULSU
- FMUL FMULS FMULSU

Data Transfer

- MOV MOVW
- LD LDI LDS LDD
- ST STS STD
- LPM ELPM
- SPM
- IN OUT
- PUSH POP

- LDI Rd, K
- LDS Rd, k
- LD Rd, X
- LD Rd, X+
- LD Rd, -X
- LDD Rd, Y+q

- LPM
- LPM Rd, Z
- LPM Rd, Z+

Bit and Bit-test

- LSL LSR
- ROL ROR
- ASR
- SWAP
- BSET BCLR
- SBI CBI
- BST BLD
- SEx CLx {C,N,Z,I,S,V,T,H}

Branch

- JMP RJMP IJMP EIJMP
- CALL RCALL ICALL EICALL
- RET RETI
- CPSE CP CPC CPI
- SBRC SBRS
- SBIC SBIS
- BREQ BRNE

Z	BREQ BRNE
C	BRCS=BRLO BRCC=BRSH
N	BRMI BRPL
N+V	BRGE BRLT
H	BRHS BRHC
T	BRTS BRTC
V	BRVS BRVC
I	BRIE BRID

MCU Control

- BREAK
- NOP
- SLEEP
- WDR