

# Fuses + Signature

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ATmega328PB





# Fuses

- „global settings“
- 3 bytes
- changes possible only from outside, when performing memory programming (can be read but cannot be changed from within MCU itself)
- not erased during Chip Erase
- 1... unprogrammed, 0 ... programmed
- cannot be changed if LB1 is set
  - ⇒ program Fuses *before* programming LB



# Fuse Low 3-0

7	6	5	4	3	2	1	0
CKDIV8	CKOUT	SUT1	SUT0	CKSEL3	CKSEL2	CKSEL1	CKSEL0

## CKSEL3-0 Clock source selection

1111 – 1000	External Low-Power Crystal
0101 – 0100	External Low-frequency Crystal
0011	Internal 128 kHz RC Oscillator
<b><u>0010</u></b>	Calibrated Internal RC Oscillator 8MHz
0000	External Clock
0001	(Reserved)



# Fuse Low 4-7

7	6	5	4	3	2	1	0
CKDIV8	CKOUT	SUT1	SUT0	CKSEL3	CKSEL2	CKSEL1	CKSEL0

**CKDIV8** Divide clock by 8

0 ... yes

1 ... no

**CKOUT** Clock output at port B pin 0

0 ... enabled

1 ... disabled

**SUT1-0** Startup time

10 (maximum)

(based on clock source)



# Fuse High 3-0

7	6	5	4	3	2	1	0
RSTDISBL	DWEN	SPIEN	WDTON	EESAVE	BOOTSZ1	BOOTSZ0	BOOTRST

**EESAVE** EEPROM behaviour during Chip Erase

0 ... preserved      1 ... erased

**BOOTSZ1-0** Boot Code size

1 1    512 B = 4 pages from 0x3F00

1 0    1024 B = 8 pages from 0x3E00

0 1    2048 B = 16 pages from 0x3C00

0 0    4096 B = 32 pages from 0x3800

**BOOTRST** Select Reset Vector

0 ... jump to Boot Loader    1 ... jump to 0x0000



# Fuse High 7-4

7	6	5	4	3	2	1	0
RSTDISBL	DWEN	SPIEN	WDTON	EESAVE	BOOTSZ1	BOOTSZ0	BOOTRST

**RSTDISBL** External Reset Disable at Port C pin 6

0 ... ext reset disabled      1 ... ext reset enabled

**DWEN** debugWire Enable

0 ... enabled      1 ... disabled

**SPIEN** Enable serial Program and Data Downloading

0 ... SPI prog. enabled      1 ... disabled

**WDTON** Watchdog Timer Always On

0 ... WDT always on      1 ... WDT controlled by  
WDTCR



# Extended Fuse

7	6	5	4	3	2	1	0
-	-	-	-	CFD	BODLEVEL 2	BODLEVEL 1	BODLEVEL 0

**CFD** Clock Failure Detection

0 ... enabled

1 ... disabled

**BODLEVEL[2:0]** Brown-Out detection level

111 ... disabled

110 ... 1.7-2.0 V (typ. 1.8)

101 ... 2.5-2.9 V (typ. 2.7)

100 ... 4.1-4.5 V (typ 4.3)

011-000 ... Reserved



# Lock Bits

- Program and Data Memory Lock Bits
- Boot Loader Lock Bits

Lock Bit Byte	Bit No.	Description	Default Value
	7	–	1 (unprogrammed)
	6	–	1 (unprogrammed)
BLB12	5	Boot lock bit	1 (unprogrammed)
BLB11	4	Boot lock bit	1 (unprogrammed)
BLB02	3	Boot lock bit	1 (unprogrammed)
BLB01	2	Boot lock bit	1 (unprogrammed)
LB2	1	Lock bit	1 (unprogrammed)
LB1	0	Lock bit	1 (unprogrammed)





# LB Mode

- General locking

Memory Lock Bits			Protection Type
LB mode	LB2	LB1	
1	1	1	No memory lock features enabled.
2	1	0	Further programming of the Flash and EEPROM is disabled in Parallel and SPI/JTAG Serial Programming mode. The Fuse bits are locked in both Serial and Parallel Programming mode. <sup>(1)</sup>
3	0	0	Further programming and verification of the Flash and EEPROM is disabled in Parallel and SPI/JTAG Serial Programming mode. The Fuse bits are locked in both Serial and Parallel Programming mode. <sup>(1)</sup>



# BLB0 Mode

- Application section protection

Memory Lock Bits			Protection Type
BLB0 mode	BLB02	BLB01	
1	1	1	No restrictions for SPM or (E)LPM accessing the Application section.
2	1	0	SPM is not allowed to write to the Application section.
3	0	0	SPM is not allowed to write to the Application section, and (E)LPM executing from the Boot Loader section is not allowed to read from the Application section. If interrupt vectors are placed in the Boot Loader section, interrupts are disabled while executing from the Application section.
4	0	1	(E)LPM executing from the Boot Loader section is not allowed to read from the Application section. If interrupt vectors are placed in the Boot Loader section, interrupts are disabled while executing from the Application section.



# BLB1 Mode

- Bootloader section protection

Memory Lock Bits			Protection Type
BLB1 mode	BLB12	BLB11	
1	1	1	No restrictions for SPM or (E)LPM accessing the Boot Loader section.
2	1	0	SPM is not allowed to write to the Boot Loader section.
3	0	0	SPM is not allowed to write to the Boot Loader section, and (E)LPM executing from the Application section is not allowed to read from the Boot Loader section. If interrupt vectors are placed in the Application section, interrupts are disabled while executing from the Boot Loader section.
4	0	1	(E)LPM executing from the Application section is not allowed to read from the Boot Loader section. If interrupt vectors are placed in the Application section, interrupts are disabled while executing from the Boot Loader section.



# Signature Row

Read only (factory-defined)

Can be read during memory programming or from the application (SPMCSR register + LPM instruction)

## DEVICEID Signature bytes

3 bytes, for ATmega328P:

\$1E (Atmel)

\$95 (32kB Flash device)

\$16 (ATmega328PB)

## RCOC Calibration byte

Automatically loaded into OSCCAL during start-up

## SERNUM Serial number

10 byte unique number

# Fuse and Lock bits reading from software



SPMCSR (Store Program Memory Control and Status Register) allows for reading Lock bits and Fuses:

\$0000 Fuse Low bits bits

\$0001 Lock bits

\$0002 Extended Fuse bits

\$0003 Fuse High bits

- Load Z-pointer with the address as above
- Set the BLBSET and SPMEN bits in SPMCSR
- LPM within 3 cycles

# Signature Row reading from software



SPMCSR (Store Program Memory Control and Status Register) allows for reading Signature Row:

\$0000,2,4	Signature
\$0001	RCOC
\$000E-17	Serial number

- Load Z-pointer with the address as above
- Set the SIGRD and SPMEN bits in SPMCSR
- LPM within 3 cycles



# Fuse and Lock bits writing

- 1 unprogrammed, 0 programmed
- Program the fuse bits *before* programming Lock bits
- Lock bits can only be erased to “1” with the Chip Erase command
- Fuses latched upon entering programming mode and stored at leave.
- Some restrictions for specific programming modes