Interrupts

generally + external interrupts

ATmega328PB

Interrupt Vector

No.	Addr.	Source	Interrupt Definition
1	*0x0000*	*RESET*	*External Pin, Power-on Reset, Brown-out Reset and Watchdog System Reset*
2	0x0002	INT0	External Interrupt Request 0
3	0x0004	INT1	External Interrupt Request 1
4	0x0006	PCINT0	Pin Change Interrupt Request 0
5	0x0008	PCINT1	Pin Change Interrupt Request 1
6	0x000A	PCINT2	Pin Change Interrupt Request 2
7	0x000C	WDT	Watchdog Time-out Interrupt
8	0x000E	TIMER2_COMPA	Timer/Counter2 Compare Match A
9	0x0010	TIMER2_COMPB	Timer/Coutner2 Compare Match B
10	0x0012	TIMER2_OVF	Timer/Counter2 Overflow
11	0x0014	TIMER1_CAPT	Timer/Counter1 Capture Event
12	0x0016	TIMER1_COMPA	Timer/Counter1 Compare Match A
13	0x0018	TIMER1_COMPB	Timer/Coutner1 Compare Match B
14	0x001A	TIMER1_OVF	Timer/Counter1 Overflow
15	0x001C	TIMER0_COMPA	Timer/Counter0 Compare Match A
16	0x001E	TIMER0_COMPB	Timer/Coutner0 Compare Match B
17	0x0020	TIMER0_OVF	Timer/Counter0 Overflow
18	0x0022	SPI0 STC	SPI1 Serial Transfer Complete
19	0x0024	USART0_RX	USART0 Rx Complete
20	0x0026	USART0_UDRE	USART0, Data Register Empty
21	0x0028	USART0_TX	USART0, Tx Complete
22	0x002A	ADC	ADC Conversion Complete

Interrupt Vector

No.	Addr.	Source	Interrupt Definition
23	0x002C	EE READY	EEPROM Ready
24	0x002E	ANALOG COMP	Analog Comparator
25	0x0030	TWI	Two-wire Serial Interface (I2C
26	0x0032	SPM READY	Store Program Memory Ready
27	0x0034	USART0_START	USART0 Start frame detection
28	0x0036	PCINT3	Pin Change Interrupt Request 3
29	0x0038	USART1_RX	USART0 Rx Complete
30	0x003A	USART1_UDRE	USART0, Data Register Empty
31	0x003C	USART1_TX	USART0, Tx Complete
32	0x003E	USART1_START	USART1 Start frame detection
33	0x0040	TIMER3_CAPT	Timer/Counter3 Capture Event
34	0x0042	TIMER3_COMPA	Timer/Counter3 Compare Match A
35	0x0044	TIMER3_COMPB	Timer/Coutner3 Compare Match B
36	0x0046	TIMER3_OVF	Timer/Counter3 Overflow
37	0x0048	CFD	Clock failure detection interrrupt
38	0x004A	PTC_EOC	PTC End of Conversion
39	0x004C	PTC_WCOMP	PTC Window comparator mode
40	0x004E	SPI1_STC	SPI1 Serial Transfer Complete
41	0x0050	TWI1	TWI1 Transfer complete
42	0x0052	TIMER4_CAPT	Timer/Counter3 Capture Event
43	0x0054	TIMER4_COMPA	Timer/Counter3 Compare Match A
44	0x0056	TIMER4_COMPB	Timer/Coutner3 Compare Match B
45	0x0058	TIMER4_OVF	Timer/Counter3 Overflow

MCU Control Register

MCUCR

7	6	5	4	3	2	1	0
	BODS	BODSE	PUD			IVSEL	IVCE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

IVSEL Interrupt Vector Select

- 0 … interrupt vector at start of program Flash
- 1 … interrupt vector at start of Boot Loader section

IVCE Interrupt Vector Change Enable

- after setting to 1, IVSEL may be changed within 4 clock cycles
- during that time, interrupts are disabled

Reset and Interrupt Vector

BOOTRST fuse	IVSEL MCUCR:1	Reset address	Interrupt Vector address
1	**0**	**$0000**	**$0002**
1	1	$0000	Boot Reset address + $0002
0	0	Boot Reset address	$0002
0	1	Boot Reset address	Boot Reset address + $0002

BOOTSZ1 fuse	BOOTSZ0 fuse	Boot Reset address	Boot Loader size
1	1	$3F00	4 pages = 256 words
1	0	$3E00	8 pages = 512 words
0	1	$3C00	16 pages = 1024 words
0	**0**	**$3800**	**32 pages = 2048 words**

ALU – Status Register

7	6	5	4	3	2	1	0
I	T	H	S	V	N	Z	C
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

I Global Interrupt Enable

T Bit Copy Storage

H Half-Carry

S Sign

V Two's Complement Overflow

N Negative

Z Zero

C Carry

MCU Control and Status Register

MCUCSR

7	6	5	4	3	2	1	0
-	-	-	-	WDRF	BORF	EXTRF	PORF
				R/W	R/W	R/W	R/W

WDRF Watchdog Reset Flag

BORF Brown-out Reset Flag

EXTRF External Reset Flag

PORF Power-on Reset Flag

INT0-1 Interrupts

EICRA

7	6	5	4	3	2	1	0
				ISC11	ISC10	ISC01	ISC00
				R/W	R/W	R/W	R/W
				0	0	0	0

ISC11-ISC10 Interrupt Sense Control 1

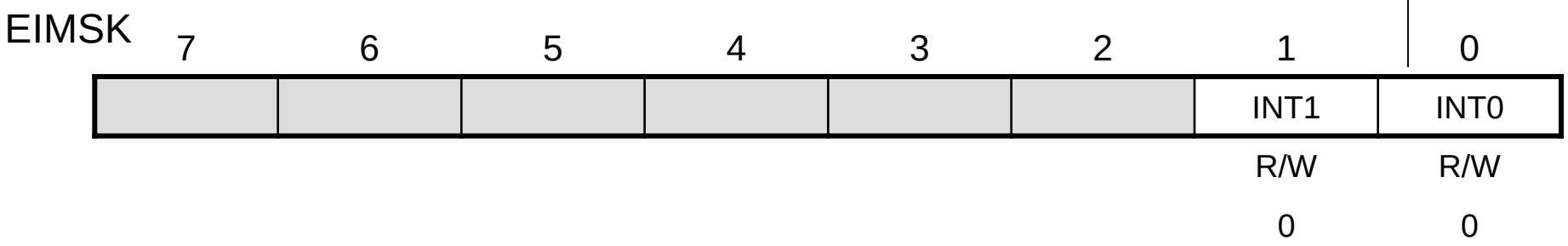
- 00 … low level
- 01 … any change
- 10 … falling edge async
- 11 … rising edge async

Level/edge event

- asynchronous regardless on the clock
  - ⇨ can wake up also from other than just Idle sleep mode
- level detected at the end of instruction execution

Multiplex PD2-PD3

External Interrupt Mask Register

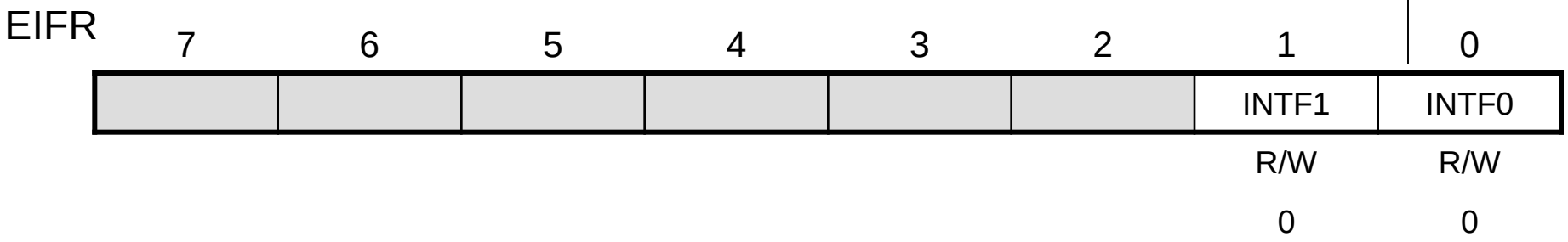


INT0-1 External Interrupt Request Enable

0 … disabled 1 … enabled

- If the conditions are met, the interrupt is called even when the pin is set to output
  - ⇨ may be used as software interrupt

External Interrupt Flag Register



INT0-1 External Interrupt Flag

0 … clear 1 … interrupt triggered

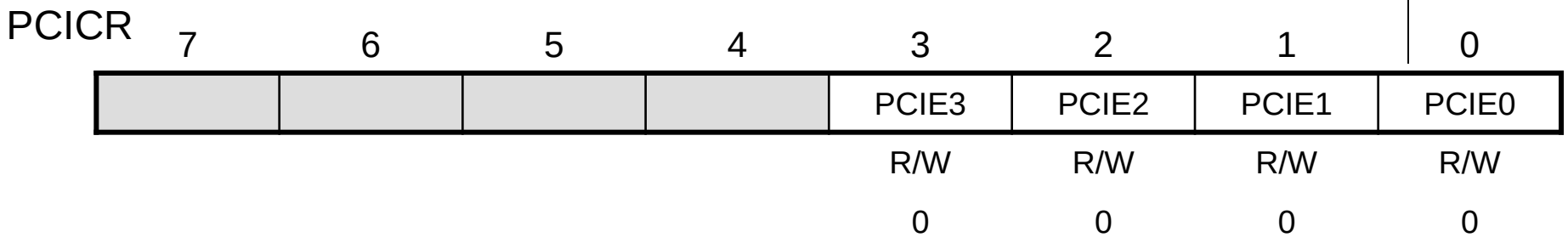
set when edge/logic change causes INT0-1

jump on the specified location

zeroed after the routine is finished (or manually)

Level interrupt ⇒ always clear

Pin Change Interrupt Control Register



PCIE0-3 Pin Change Interrupt Enable

0 … disabled 1 … enabled

Pin Change Interrupt Flag Register

PCIFR

7	6	5	4	3	2	1	0
				PCIF3	PCIF2	PCIF1	PCIF0
				R/W	R/W	R/W	R/W
				0	0	0	0

PCIF0-3 Pin Change Interrupt Flag

0 … clear 1 … interrupt triggered

set when logic change causes PCINT0-3

jump on the specified location

zeroed after the routine is finished (or manually)

Level interrupt $\Rightarrow$ always clear

Pin Change Mask Register 3

PCMSK3

PCMSK2

PCMSK1

PCMSK0

7	6	5	4	3	2	1	0
				PCINT27	PCINT26	PCINT25	PCINT24
PCINT23	PCINT22	PCINT21	PCINT20	PCINT19	PCINT18	PCINT17	PCINT16
	PCINT14	PCINT13	PCINT12	PCINT11	PCINT10	PCINT9	PCINT8
PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

PCINT0-27 Pin Change Interrupt Enable Mask

0 … disabled 1 … enabled

Pin Change Interrupt Pins

PCINT0-7	Port B (0-7)
PCINT8-14	Port C (0-6)
PCINT16-23	Port D (0-7)
PCINT24-27	Port E (0-3)