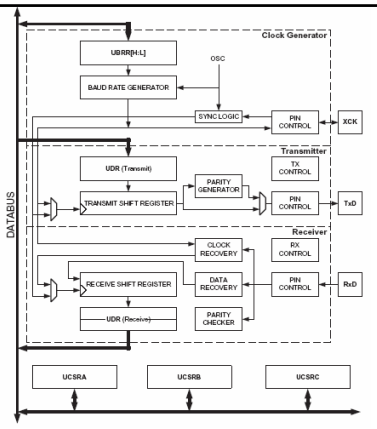
USART

ATmega8

Universal Synchronous and Asynchronous serial Receiver and Transmitter

- full duplex
- synchronní nebo asynchronní provoz
- synchronní master/slave
- 5,6,7,8,9 data bits + 1,2 stop bits
- sudá/lichá parita, parity check v HW
- Interrupty: TX complete, TX DRE, RX complete



Clock Mode

- normal asynchronous
- double asynchronous
- master synchronous
- slave synchronous

Baud rate

- USART Baud Rate Register (UBRR)

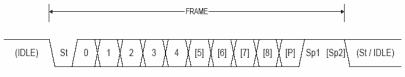
Table 52. Equations for Calculating Baud Rate Register Setting

Operating Mode	Equation for Calculating Baud Rate[1]	Equation for Calculating UBRR Value
Asynchronous Normal mode (U2X = 0)	$BAUD = \frac{f_{OSC}}{16(UBRR+1)}$	$UBRR = \frac{f_{OSC}}{16BAUD} - 1$
Asynchronous Double Speed Mode (U2X = 1)	$BAUD = \frac{f_{OSC}}{8(UBRR+1)}$	$UBRR = \frac{f_{OSC}}{8BAUD} - 1$
Synchronous Master Mode	$BAUD = \frac{f_{OSC}}{2(UBRR+1)}$	$UBRR = \frac{f_{OSC}}{2BAUD} - 1$

- Slave - externí

Frames

- 1 start bit
- 5-9 data bits
- no/odd/even parity
- 1-2 stop bits
- UCSRB, UCSRC (UCSZ2:0, UPM1:0 and USBS bits)



USART
Control and Status Register A

UCSRA

7	6	5	4	3	2	1	0
RXC	TXC	UDRE	FE	DOR	PE	U2X	MPCM
R	R/W	R	R	R	R	R/W	R/W
0	0	1	0	0	0	0	0

RXC USART Receive Complete
TXC USART Transmit Complete
UDRE USART Data Register Empty
FE Frame Error
DOR Data OverRun
PE Parity Error
U2X USART Double Transmission Speed
MPCM Multi-Processor Communication Mode

USART
Control and Status Register B

UCSRB

7	6	5	4	3	2	1	0
RXCIE	TXCIE	UDRIE	RXEN	TXEN	UCSZ2	RXB8	TXB8
R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
0	0	0	0	0	0	0	0

RXCIE RX Complete Interrupt Enable
TXCIE TX Complete Interrupt Enable
UDRIE Data Register Empty Interrupt Enable
RXEN Receiver Enable
TXEN Transmitter Enable
UCSZ2 Character Size
RXB8 Receive Data Bit 8
TXB8 Transmit Data Bit 8

USART
Control and Status Register C

UCSRC

7	6	5	4	3	2	1	0
URSEL	UMSEL	UPM1	UPM0	USBS	UCSZ1	UCSZ0	UCPOL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	0	0	0	1	1	0

URSEL Register Select
UMSEL USART Mode Select
UPM1:0 Parity Mode
USBS Stop Bit Select
UCSZ1:0 Character Size
UCPOL Clock Parity

UBRRH, UBRRL

UBRRH

7	6	5	4	3	2	1	0
URSEL	-	-	-	UBRR11:8			
R/W	R	R	R	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

UBRRL

7	6	5	4	3	2	1	0
UBRRL7:0							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

URSEL Register Select
UBBR11:0 USART Baud Rate Register

USART
I/O Data Register

UDR

7	6	5	4	3	2	1	0
RXB7:0 / TXB7:0							
R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
0	0	0	0	0	0	0	0