Interrupts

ATmega128

Interrupt Vector

No.	Addr.	Source	Interrupt Definition
1	*0x0000*	*RESET*	*External Pin, Power-on Reset, Brown-out Reset, and Watchdog Reset*
2	0x0002	INT0	External Interrupt Request 0
3	0x0004	INT1	External Interrupt Request 1
4	0x0006	INT2	External Interrupt Request 2
5	0x0008	INT3	External Interrupt Request 3
6	0x000A	INT4	External Interrupt Request 4
7	0x000C	INT5	External Interrupt Request 5
8	0x000E	INT6	External Interrupt Request 6
9	0x0010	INT7	External Interrupt Request 7
10	0x0012	TIMER2 COMP	Timer/Counter2 Compare Match
11	0x0014	TIMER2 OVF	Timer/Counter2 Overflow
12	0x0016	TIMER1 CAPT	Timer/Counter1 Capture Event
13	0x0018	TIMER1 COMPA	Timer/Counter1 Compare Match A
14	0x001A	TIMER1 COMPB	Timer/Counter1 Compare Match B
15	0x001C	TIMER1 OVF	Timer/Counter1 Overflow
16	0x001E	TIMER0 COMP	Timer/Counter0 Compare Match

Interrupt Vector

No.	Addr.	Source	Interrupt Definition
17	0x0020	TIMER0 OVF	Timer/Counter0 Overflow
18	0x0022	SPI, STC	Serial Transfer Complete
19	0x0024	USART0, RX	USART0, Rx Complete
20	0x0026	USART0, UDRE	USART0 Data Register Empty
21	0x0028	USART0, TXC	USART0, Tx Complete
22	0x002A	ADC	ADC Conversion Complete
23	0x002C	EE READY	EEPROM Ready
24	0x002E	ANALOG COMP	Analog Comparator
25	0x0030	TIMER1 COMPC	Timer/Counter1 Compare Match C
26	0x0032	TIMER3 CAPT	Timer/Counter3 Capture Event
27	0x0034	TIMER3 COMPA	Timer/Counter3 Compare Match A
28	0x0036	TIMER3 COMPB	Timer/Counter3 Compare Match B
29	0x0038	TIMER3 COMPC	Timer/Counter3 Compare Match C
30	0x003A	TIMER3 OVF	Timer/Counter3 Overflow
31	0x003C	USART1, RX	USART1, Rx Complete
32	0x003E	USART1, UDRE	USART1 Data Register Empty
33	0x0040	USART1, TXC	USART1, Tx Complete
34	0x0042	TWI	Two-wire Serial Interface
35	0x0044	SPM_RDY	Store Program Memory Ready

MCU Control Register

MCUCR

7	6	5	4	3	2	1	0
SRE	SRW10	SE	SM1	SM0	SM2	IVSEL	IVCE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

IVSEL Interrupt Vector Select

- 0 … interrupt vector at start of program Flash
- 1 … interrupt vector at start of Boot Loader section

IVCE Interrupt Vector Change Enable

- after setting to 1, IVSEL may be changed within 4 clock cycles
- during that time, interrupts are disabled

Reset and Interrupt Vector

BOOTRST fuse	IVSEL MCUCR:1	Reset address	Interrupt Vector address
1	**0**	**$0000**	**$0002**
1	1	$0000	Boot Reset address + $0002
0	0	Boot Reset address	$0002
0	1	Boot Reset address	Boot Reset address + $0002

BOOTSZ1 fuse	BOOTSZ0 fuse	Boot Reset address
1	1	$FE00
1	0	$FC00
0	1	$F800
0	**0**	**$F000**

INT0-3 - External Interrupts

EICRA

7	6	5	4	3	2	1	0
ISC31	ISC30	ISC21	ISC20	ISC11	ISC10	ISC01	ISC00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

ISC11-ISC10 Interrupt Sense Control 1

- 00 … low level
- 01 … reserved
- 10 … falling edge async
- 11 … rising edge async

Level/edge event

- asynchronous regardless on the clock
  - ⇨ can wake up also from other than just Idle sleep mode
- level detected at the end of instruction execution

Multiplex PD0-PD3

INT4-7 - External Interrupts

EICRB

7	6	5	4	3	2	1	0
ISC71	ISC70	ISC61	ISC60	ISC51	ISC50	ISC41	ISC40
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

ISC11-ISC10 Interrupt Sense Control 1

00 … low level 10 … falling edge

01 … any change 11 … rising edge

Level event

asynchronous regardless on the clock

⇨ can wake up also from other than just Idle sleep mode

level detected at the end of instruction execution

Edge/toggle event

depends on the clock, pulse must be longer than 1 clock

Multiplex PE4-PE7

External Interrupt Mask Register

EIMSK

7	6	5	4	3	2	1	0
INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

INT0-7 External Interrupt Request Enable

0 … disabled 1 … enabled

- If the conditions are met, the interrupt is called even when the pin is set to output
  - ⇨ may be used as software interrupt

External Interrupt Flag Register

EIFR

7	6	5	4	3	2	1	0
INTF7	INTF6	INTF5	INTF4	INTF3	INTF2	INTF1	INTF0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

INT0-7 External Interrupt Flag

0 … clear 1 … interrupt triggered

set when edge/logic change causes INT0-7

jump on the specified location

zeroed after the routine is finished (or manually)

Level interrupt ⇒ always clear