I²C, SMBus, TWI

Atmel AVR Core

I²C bus

- Two-wire (SDA, SCL)
- Open-drain design (pull-ups needed)
  - Dominant: low level, Recessive: high level
  - +5V or +3.3V typically (other voltages permitted)
- Definition includes low level, collisions, data format, acknowledgements, control
- Master/slave control
- Multi-master configuration possible
- 0- 100/400/1000/3400/5000 kHz clock

www.philipslogic.com/i2c

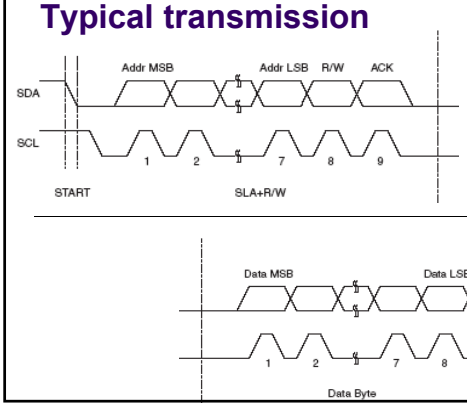
SMBus (SMB)

- defined by Intel in 1995
- subset of I²C
- more strict protocol
  - any format vs. 9 message structures
  - limits on clock stretching
  - slave arbitration

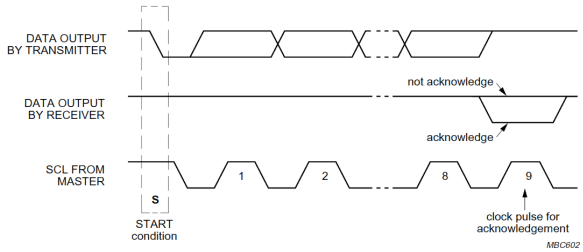
TWI

- Two-wire interface by Atmel
- until 2006 licence fees required to implement I²C protocol
  - since 2006 only slave address allocation for fee

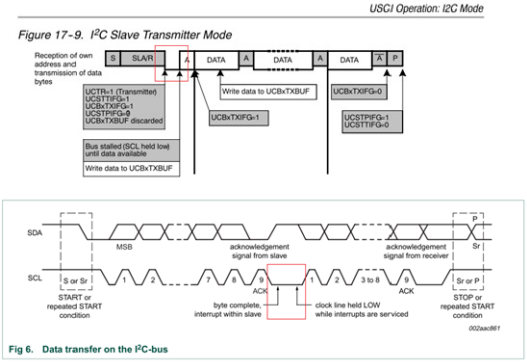
Typical transmission



Transmission acknowledgement



Clock stretching

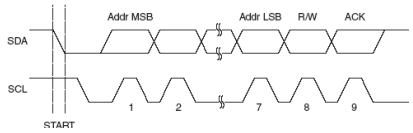


Message protocols

- Single write master ⇨ slave
- Single read master ⇦ slave
- Combined, at least 2 master-slave reads/writes

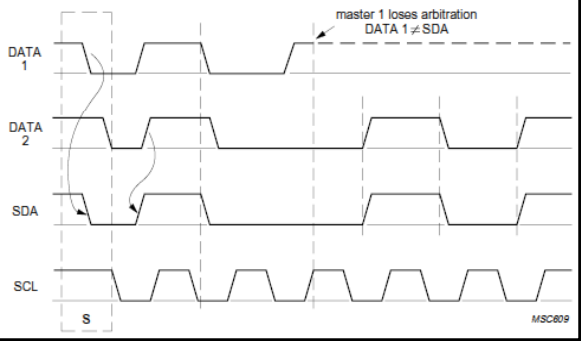
- all begin with START condition
- all end with STOP condition

Addressing



- 7bit (+ r/w + ack)
- 0000 000 “general call”
- 1111 xxx reserved for future use

Multi-master arbitration



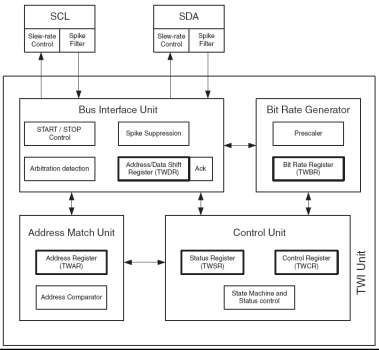
Applications

- Low-speed communication of any kind
  - configuration management
    - SPD EEPROMs – SDRAM, DDR, DDR2 etc.
    - DDC – VGA, DVI, HDMI, DisplayPort
  - DAC / ADC
  - hardware monitoring
  - small display drivers
  - RTC
  - power control applications
  - …

OS Support

- All major OSs:
  - Mac OS X
  - MS Windows
  - Linux
  - RISC OS
- Many many small systems
  - Arduino
  - Picaxe
  - AmigaOS
  - …. ……

AVR TWI Module



$$\text{SCL frequency} = \frac{\text{CPU Clock frequency}}{16 + 2(\text{TWBR}) \cdot 4^{TWPS}}$$

- Byte oriented, interrupt based
  - interrupts after all bus events
- TWBR, TWCR, TWSR, TWDR, TWAR

TWI Bit Rate Register

TWBR

7	6	5	4	3	2	1	0
TWBR7							TWRB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

TWRB7:0 bit rate generator division factor

TWI Control Register

TWCR

7	6	5	4	3	2	1	0
TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	-	TWIE
R/W	R/W	R/W	R/W	R	R/W	R	R/W
0	0	0	0	0	0	0	0

TWINT TWI Interrupt Flag
TWEA TWI Enable Acknowledge Bit
TWSTA TWI START Condition Bit
TWSTO TWI STOP Condition Bit
TWWC TWI Write Collision Flag
TWEN TWI Enable Bit
TWIE TWI Interrupt Enable

TWSR TWI Status Register

TWSR

7	6	5	4	3	2	1	0
TWS7	TWS6	TWS5	TWS4	TWS3	-	TWPS1	TWPS0
R	R	R	R	R	R	R/W	R/W
1	1	1	1	1	0	0	0

TWS7:3 TWI Status Code
TWPS1:0 TWI Prescaler Bits

TWDR TWI Data Register

TWDR

7	6	5	4	3	2	1	0
TWD7							TWD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

TWD7:0 TWI Data

TWAR TWI (Slave) Address Register

TWAR

7	6	5	4	3	2	1	0
TWA6						TWA0	TWGCE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	0

TWA6:0 TWI TWI (Slave) Address Register
TWGCE TWI General Call Recognition Enable Bit