

Sleep

Atmel ATmega128



Configuration

- MCUCR

7	6	5	4	3	2	1	0
SRE	SRW10	SE	SM1	SM0	SM2	IVSEL	IVCE
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

SM2	SM1	SM0	Sleep Mode
0	0	0	Idle
0	0	1	ADC Noise Reduction
0	1	0	Power-down
0	1	1	Power-save
1	0	0	(reserved)
1	0	1	(reserved)
1	1	0	Standby
1	1	1	Extended Standby

- SLEEP instruction stops the CPU

Idle Mode

- peripherals keep running
 - SPI, USART, Analog Comparator, ADC, TWI, Timers/counters, Watchdog, Interrupts
 - technically: stops clk_{CPU} , clk_{FLASH}
- ADC will start once the CPU has been halted

ADC Noise Reduction Mode

- some peripherals keep running
 - ADC, External Interrupts, TWI address watch, Timer/Counter0, Watchdog
 - technically: stops clk_{CPU} , $clk_{I/O}$, clk_{FLASH}
- ADC will start once the CPU has been halted
- Waking interrupts
 - External Reset, Watchdog, Brown-out Reset
 - TWI address match
 - SPM/EEPROM ready
 - External Level IRQ 7:4, External IRQ 3:0
 - Timer/Counter0

Power-Down Mode

- only asynchronous modules keep running
 - External Interrupts, TWI address watch, Timer/Counter0, Watchdog
 - technically: stops all clocks
- Waking interrupts
 - External Reset, Watchdog, Brown-out Reset
 - TWI address match
 - External Level IRQ 7:4, External IRQ 3:0
- Wake-up period defined by CKSEL fuses

Power-save Mode

- nearly power-down, except:
 - if Timer/Counter0 is asynchronous, device can wake up from Timer Overflow or Output Compare
 - if Timer/Counter0 is NOT asynchronous, registers are undefined after wake-up
 - technically: stops all clocks except clk_{ASY}

Standby Mode

- nearly power-down, but
 - Oscillator is running
 - Device wakes up in 6 clock cycles



Extended Standby Mode

- nearly power-save, but
 - Oscillator is running
 - Device wakes up in 6 clock cycles



Summary

Table 18. Active Clock Domains and Wake Up Sources in the Different Sleep Modes

Sleep Mode	Active Clock Domains					Oscillators		Wake Up Sources					
	clk _{CPU}	clk _{FLASH}	clk _{IO}	clk _{ACC}	clk _{AEV}	Main Clock Source Enabled	Timer Osc Enabled INT7:0	TWI Address Match	Timer 0	SPM/EEPROM Ready	ADC	Other I/O	
Idle			X	X	X	X	X ⁽²⁾	X	X	X	X	X	X
ADC Noise Reduction				X	X	X	X ⁽²⁾	X ⁽³⁾	X	X	X	X	
Power-down								X ⁽³⁾	X				
Power-save					X ⁽²⁾		X ⁽²⁾	X ⁽³⁾	X	X ⁽²⁾			
Standby ⁽¹⁾						X		X ⁽³⁾	X				
Extended Standby ⁽¹⁾					X ⁽²⁾	X	X ⁽²⁾	X ⁽³⁾	X	X ⁽²⁾			

Notes: 1. External Crystal or resonator selected as clock source
 2. If ASD bit in ASSR is set
 3. Only INT3:0 or level interrupt INT7:4

