Programování mikrokontrolerů

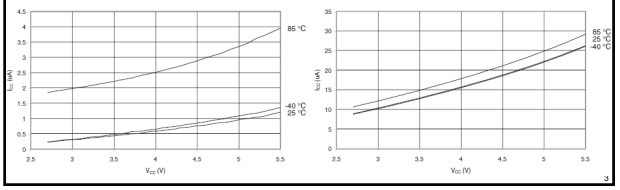
AVR Watchdog

General info

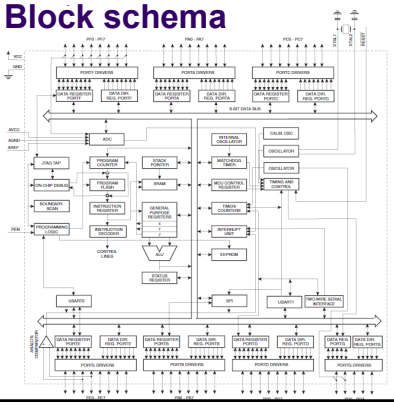
- Peripheral features
  - …
  - Programmable Watchdog Timer with On-Chip Oscillator
  - …
- Reset sources
  - …
  - Watchdog Reset. The MCU is reset when the Watchdog Timer period expires and the Watchdog is enabled.
  - …

General info

- If enabled, Watchdog is active in all sleep modes
  - … and draws current, which contributes significantly to the total power consumption in deep sleep modes.



AVR Block schema



AVR Clock System

Figure 18. Clock Distribution

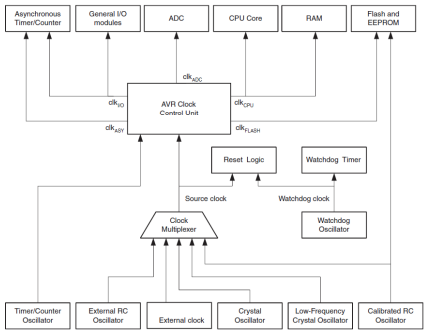
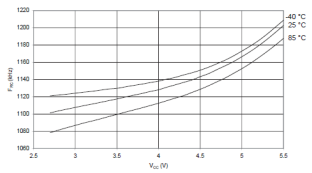


Table 7. Number of Watchdog Oscillator Cycles

Typical Time-out (V_{CC} = 5.0V)	Typical Time-Out (V_{CC} = 3.0V)	Number of Cycles
4.1ms	4.3ms	4K (4,096)
65ms	69ms	64K (65,536)

Figure 192. Watchdog Oscillator Frequency vs. V_{CC}



MCU Control and Status Register

MCUCSR

7	6	5	4	3	2	1	0
JTD	-	-	JTRF	WDRF	BORF	EXTRF	PORF
R/W	R	R	R/W	R/W	R/W	R/W	R/W
0	0	0					

JTD JTAG Interface Disable
JTRF JTAG Reset Flag
WDRF Watchdog Reset Flag
BORF Brown-out Reset Flag
EXTRF External Reset Flag
PORF Power-on Reset Flag

WDTCR
Watchdog Timer Control Register

WDTCR

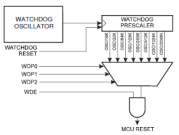
7	6	5	4	3	2	1	0
-	-	-	WDCE	WDE	WDP2	WDP1	WDP0
R	R	R	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

WDCE Watchdog Change Enable
WDE Watchdog Enable
WDP2:0 Watchdog Timer Prescaler

Table 22. Watchdog Timer Prescale Select

WDP2	WDP1	WDP0	Number of WDT Oscillator Cycles
0	0	0	16K (16,384)
0	0	1	32K (32,768)
0	1	0	64K (65,536)
0	1	1	128K (131,072)
1	0	0	256K (262,144)
1	0	1	512K (524,288)
1	1	0	1,024K (1,048,576)
1	1	1	2,048K (2,097,152)

Figure 28. Watchdog Timer



Extended Fuse

7	6	5	4	3	2	1	0
-	-	-	-	-	-	M103C	WDTON

M103C ATmega103 compatibility mode
0 … ON 1 … OFF
WDTON Watchdog control
0 … WDT always on **1** … WDTCR controls WDT

Table 21. WDT Configuration as a Function of the Fuse Settings of M103C and WDTON.

M103C	WDTON	Safety Level	WDT Initial State	How to Disable the WDT	How to Change Time-out
Unprogrammed	Unprogrammed	1	Disabled	Timed sequence	Timed sequence
Unprogrammed	Programmed	2	Enabled	Always enabled	Timed sequence
Programmed	Unprogrammed	0	Disabled	Timed sequence	No restriction
Programmed	Programmed	2	Enabled	Always enabled	Timed sequence

Timed Sequences and Safety Levels

- SL0
  - WDT initially disabled, can be enabled without restriction
  - Timeout can be changed without restriction
  - Disabled using *the* timed sequence
- SL1
  - WDT initially disabled, can be enabled without restriction
  - Timeout changed and/or WDT disabled using *the* timed sequence

10

Timed Sequences and Safety Levels

- SL2
  - WDT always enabled, WDE always read 1
  - Timeout changed using *the* timed sequence

11

WDR – Watchdog Reset

Description:

This instruction resets the Watchdog Timer. This instruction must be executed within a limited time given by the WD prescaler. See the Watchdog Timer hardware specification.

Operation:
(i) WD timer restart.

Syntax: (i) WDR
Operands: None
Program Counter: PC ← PC + 1

16-bit Opcode:

1001	0101	1010	1000

Status Register and Boolean Formula:

I	T	H	S	V	N	Z	C
–	–	–	–	–	–	–	–

Example:

```
wdr       ; Reset watchdog timer
```

Words: 1 (2 bytes)
Cycles: 1

12